cipher data products, inc.

M990 GCR
CacheTape®

M990 GCR
CacheTape® Unit
Theory of Operation

Technical Manual
No. 799891-002
Third Edition

Federal Communications Commission (FCC) Notice

Warning: This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instruction manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

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CHAPTER 1.

1.1 DESCRIPTION

Physical Description

The GCR CacheTape* Unit (GCR) is a nine-track, multi-density, tape transport manufactured by Cipher Data Products, Inc., San Diego, California. The unit is designed to be rack-mounted in a standard 19-inch equipment rack. All components are mounted on a precision-machined, cast aluminum plate. When the equipment rack is securely anchored, the PWB and other internal components can be made accessible from the front by releasing the equipment latch located inside the front panel (bottom) and pulling the unit forward on slides.

The GCR simulates traditional tape drives by means of an internal cache memory that performs the logical functions of a physical drive. The host system interfaces directly with the logical drive. Data records from the host are stored in cache memory and then written on tape by the physical drive, independent of the host. The physical drive is thus virtually transparent to the host system.

There is one GCR model: the Model M990. It records at 1600, 3200, and 6250 bytes-per-inch (BPI). The M990 has a maximum data transfer rate of 632 kilobytes-per-second (KBS) and has built-in start delays to simulate the physical tape ramp time of conventional start/stop transports.

There are two different access positions for the unit. The first position, operator maintenance access, provides accessibility to the supply reel, head, and tape roller guides. The second position, service access, provides access to all electronic components as well as mechanical parts.

Physical Tape Drive Mechanism

The reel-to-reel drive mechanism employs two direct-drive, dc, torque motors to drive the tape reels. An optical tachometer assembly on the takeup hub regulates tape speed. Tape tension is maintained at approximately 9 ounces by a single tension arm.

The tape path includes roller guides, a dual-gap head, and a tape cleaner. All roller guides incorporate precision bearings to minimize friction and wear. The roller guides, positioned on both sides of the head, utilize polished ceramic washers to guide the tape across the head. This arrangement minimizes skew and the effect of tape-width variations.

A tape cleaner is mounted adjacent to the head to minimize tape contamination.

Functional Description

Figure 1-1 is a system block diagram. The GCR can be functionally divided into the logical tape unit and the physical tape unit, both of which are controlled by the Z8002 microprocessor. The logical unit consists of the cache memory and associated logic circuits, while the physical unit consists of the read/write circuits, read/write head, the physical drive mechanisms, and the related sensing and controlling devices. The DMA controller, under the overall control of the microprocessor, directly controls the cache memory.

The microprocessor is supported by 64K of control storage (EPROM) and two 64K sets of dynamic random access memories (DRAMs). The microprocessor also has analog input and output ports for diagnostic purposes, control of motor drivers, and read threshold selection.

The interface logic in the GCR consists of the following:

a. Read/write latches and strobes.

b. Command and status latches.

The read/write latches and strobe logic are connected to the DMA controller and cache memory through device request logic. The microprocessor determines the rate of access. The command and status latches interface directly with the microprocessor logic. The host interface communicates only with the logical tape drive.

Cache memory is 256KB of DRAMs. The memory is logically a circular buffer and is addressed by the DMA controller. The three channels of the DMA controller perform the following services in the priority listed:

a. Physical tape drive

b. Logical tape drive

c. Microprocessor

The write formatter is under the direct control of the microprocessor. The ID burst, preamble, postamble, and file mark are generated internally by the formatter. The formatter output is sent to the write electronic circuits, which drive the physical tape drive head to write the formatted data on the tape.

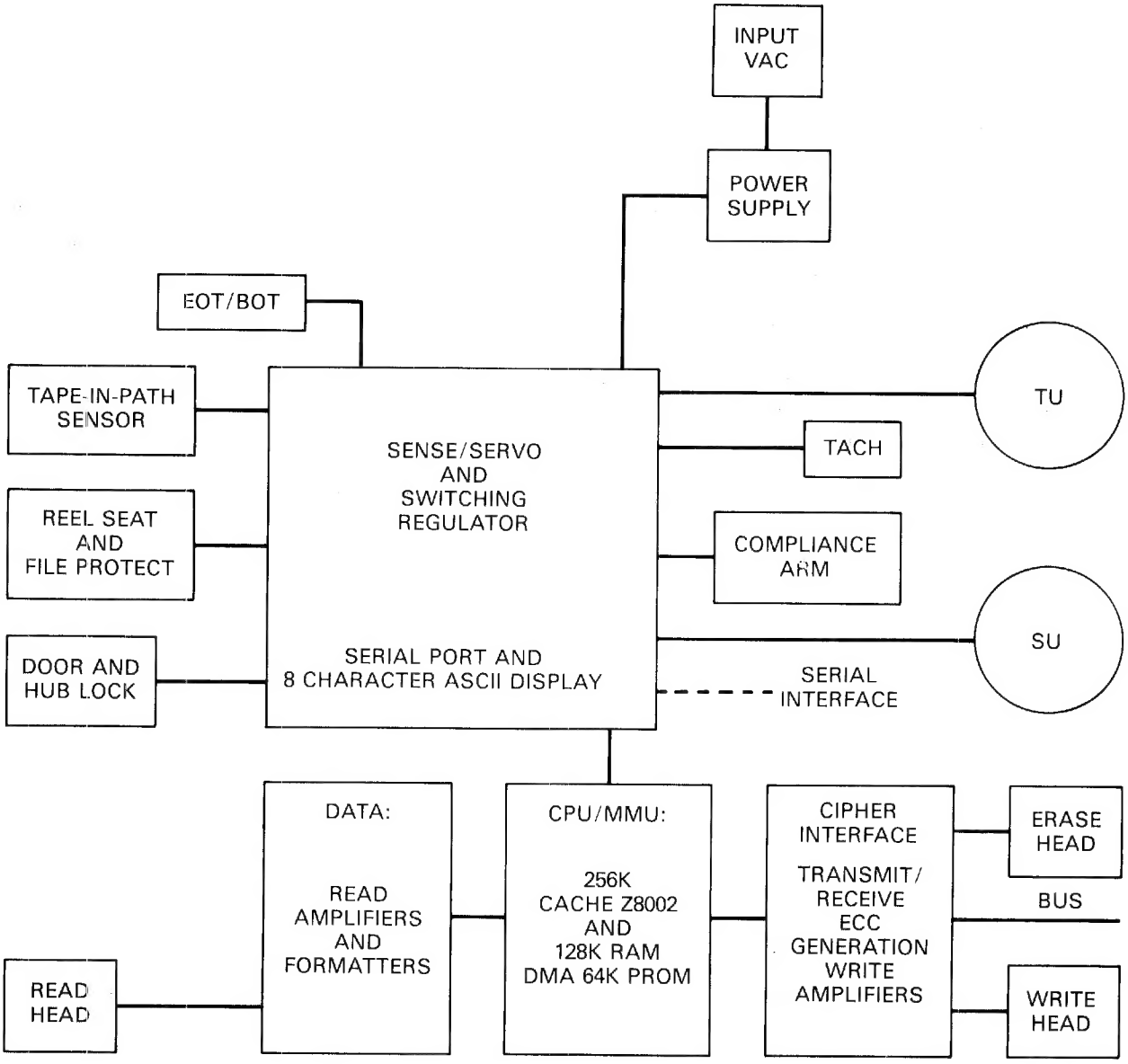


Figure 1.1 System Block Diagram

During a read operation, the read electronic circuits recover the low-voltage read signals from the read head, condition the signals, and route the signals to the read formatter. The read formatter detects the polarity of the data transitions and sends input requests to the serial processing and skew buffer in the read formatter logic. When a full data character is assembled by the skew buffer, the buffer requests that the DMA controller recover the character and place it in cache memory.

Tape movement in the physical tape drive is controlled primarily by the takeup servo and tachometer assembly. The velocity information generated by the tachometer assembly is used to develop the drive voltage for the takeup motor. The tachometer is also used to derive position displacement information between the beginning and end of consecutive tape records.

The supply motor is the driving mechanism of a position servo loop that maintains the tape at the proper tension. The compliance arm is held at a position between its two limit stops. Any tape movement causes a change in position of the compliance arm, resulting in a feedback signal from the compliance arm position sensor to the supply reel servo. The servo adjusts the supply reel motor speed and direction to correct the compliance arm position.

The end-of-tape (EOT) and beginning-of-tape (BOT) sensors consist of two infrared LEDs and detectors operating on reflections from ANSI metallized markers applied to standard tape reels.

An infrared detector adjacent to the supply reel senses that the tape is in the tape path. This ensures reliable tape loading.

1.2 SPECIFICATIONS

Interface Specifications

Signal characteristics are as follows:

a. Levels

(1) True is low: 0 to +0.4 volt (approximately).
(2) False is high: +3.0 volts (approximately).

b. Pulses

(1) Levels as above.
(2) Edge transmission delay over 25 feet of cable is not greater than 200 nanoseconds.

The interface circuits are so designed that a disconnected wire results in a false signal. Figure 1-2 shows the interface configuration for which the transport is designed.

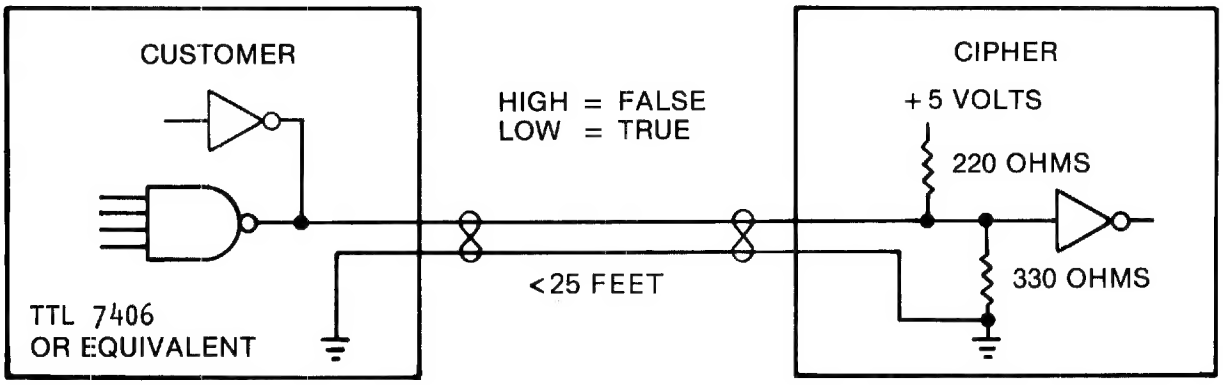


Figure 1-2. Interface Configuration

Mechanical and Electrical Specifications

Recording Method	Phase Encoded (PE) Group Code Recording (GCR)
Data Tracks	8
Parity Tracks	1
Density	1600 BPI 3200 BPI 6250 BPI
Physical Tape Speeds	100 IPS (PE) 50 IPS (3200 BPI) 70 IPS (GCR)
Reposition Time	1.080 sec (PE) 0.540 sec (3200 BPI) 0.743 sec (GCR)
I/F Character Rate (burst mode)	70.3-632 kbs (burst mode)

Physical Dimensions

Height	14.0 in. (35.56 cm)
Width	17.0 in. (43.18 cm)
Depth (from mounting surface)	22.0 in. (55.88 cm)
Overall Depth	24.5 in. (62.23 cm)
Weight	100 lbs (43.36 kg)

Environmental

Operating*:

Dry Bulb Temperature	10^{o} to 40^{o}C
Wet Bulb Temperature	26^{o}C max
Relative Humidity	20-85% (non-condensing)
Barometric Pressure	20" Hg to 35" Hg (68 kPa to 119 kPa)
Altitude	Sea level to 10,000 ft (3km)
Temperature Shock	1^{o}C/min (max)
Generated Heat	1300 BTU/hour max (vented to enclosure)
Acoustic Noise	60 DBA max

* The ambient temperature must be maintained within ANSI media limits to ensure the data integrity of the media. The ANSI max is 32 degrees centigrade.

Non-operating (Long Term):

Dry Bulb Temperature	-40^{o} to 50^{o}C
Wet Bulb Temperature	30^{o}C max
Relative Humidity	90% max non-condensing
Altitude	Sea level to 10,000 ft (3km)

Shipping and Short Term Storage:

Dry Bulb Temperature	-40^{o} to 70^{o}C
Wet Bulb Temperature	40^{o}C max
Relative Humidity	95% max non-condensing
Altitude	Sea level to 49,000 ft (15km)

Tape Speed (Determined by density)

100 IPS (1600 BPI)
70 IPS (6250 BPI)
50 IPS (3200 BPI)

Long Term Speed Variation (LSV)	±1% of nominal
Instantaneous Speed Variation (ISV)	±2% of long term

Rewind Time	110 sec nominal-150 sec max

Recording Density	
GCR	6250 CPI or 9042 FRPI
PE	1600 CPI or 3200 FRPI
PE	3200 CPI or 6400 FRPI
Error Correction	
GCR	2 channel (read)
PE	1 channel (read)
Erase Gap	4.2 in.
Data Format	
GCR	Compatible with ANSI STD X3.54 - 1976
PE	Compatible with ANSI STD X3.39 - 1973
Block Size (max)	32 K bytes
Cache Memory	256 K bytes
Tape Computer Grade	ANSIX3.40 - 1976
Width	0.5 in.
Thickness	1.5 milli-inch substrate
Reel Size	7 in., 8.5 in., or 10.5 in.
Tape Tension	9.5 oz. nominal

Data Reliability (errors other than media faults)

	For PE	For GCR
Write	1 error in 10^8 bytes	1 error in 10^8 bytes
Read Recoverable	1 error in 10^9 bytes	1 error in 10^{10} bytes
Read Permanent	1 error in 10^{10} bytes	1 error in 10^{11} bytes

MTBF (20% duty cycle)	5440 hours
MTTR (to isolate and replace major assemblies)	30 minutes

Inter-record Gap

	For PE	For GCR
	0.6 in. (at 1600/3200 BPI) nominal	0.3 in. nominal
	0.5 in. min	0.28 in. min
	25 ft. max	15 ft. max

Formatter Interface	Industry compatible Cipher standard
Interface Impedance	110 ohms a 3 Vdc
Logic Low	0.4 Vdc, max
Logic High	2.4 Vdc, min
Rise/Fall Time	100 nanoseconds, max
Cable Characteristics	22 or 24 AWG twisted pair (shielded)

Input Power and Grounding

Operating Frequency	
Frequency	49 to 61 Hz
Rate of Change	1.5 Hz/sec, max
Utilization Voltage	
Nominal input voltage (slow-averaged rms, including brownouts)	100, 104, 110, 120, 127, 200, 208 220, 230,240
Range of nominal voltage except 208, 230	±10%, -15%
Range of nominal 208, 230 voltage	±10%, -10%
Modulation	1%, max
Harmonics (total)	10%, max
Power Consumption	500VA max 400W max at 0.85 pf 250 W operating at 0.85 pf

DIGITAL RECORDING TECHNIQUES

CHAPTER 2.

2.1 GENERAL

The basic concepts of digital recording, magnetic tape transport applications, and principles of operation of the GCR CacheTape* Unit (GCR) are presented in this section. A thorough knowledge of this section will be of considerable value in troubleshooting this equipment.

Basic Concepts of Digital Recording

The use of magnetic tape as a digital recording medium has increased steadily as a result of the increased use of microprocessor technology and the increasing versatility and decreasing cost of tape transports. The digital recording process involves methods and equipment capable of recording and reading information expressed in digital (binary) code.

Data Recording/Reading With Magnetic Tape

The recording of data on magnetic tape originates with the input device, whose nine channels of digital signals are transmitted to the corresponding data channels of the transport in parallel bytes composed of nine bits aligned across the width of the magnetic tape. A bit is a binary 1 or 0 which is presented in magnetic tape recording by the presence or absence of a flux reversal, or by a plus or minus direction of flux reversal, depending upon the coding system. (One of these channels is the parity channel, which is used to correct errors which occur when one of the other eight bits is not properly recovered). These signals produce corresponding electrical currents in the read head of the transport, which, in turn, produces positive and negative magnetic polarities corresponding to the original data and parity signals in the tracks of the tape passing over it. The details of the methods in which the data is recorded for phase-encode (PE) and group code recording (GCR) are given in the respective descriptions in this section.

2.2 GROUP CODE RECORDING

Group Code Recording (GCR) is used for 6250 bits per inch (BPI) in the nine-track mode. The major advantage offered by the GCR format is high density with optimum data integrity, including enhanced error detection/correction facilities.

The GCR method uses the Non-Return-Zero (NRZI) Change on Ones recording technique and is formatted in the GCR structure.

NRZI Recording Technique

The NRZI system, recording is carried out by a saturation current driven through the head in a direction determined by a flip-flop which toggles for each 1 bit recorded. The NRZI system requires the recording of at least one bit for every character; otherwise, in an all-O character there would be no indication of the presence of that character. When O's are written in all eight data tracks, the required one bit is written in the parity track. The basic features of the NRZI system are as follows:

a. At data time, no change in magnetic tape polarity means a O bit.

b. A change from negative to positive or positive to negative is a bit.

c. There is no change of polarity between data bits.

See Figure 2-1 for description of NRZI-type writing and reading signals.

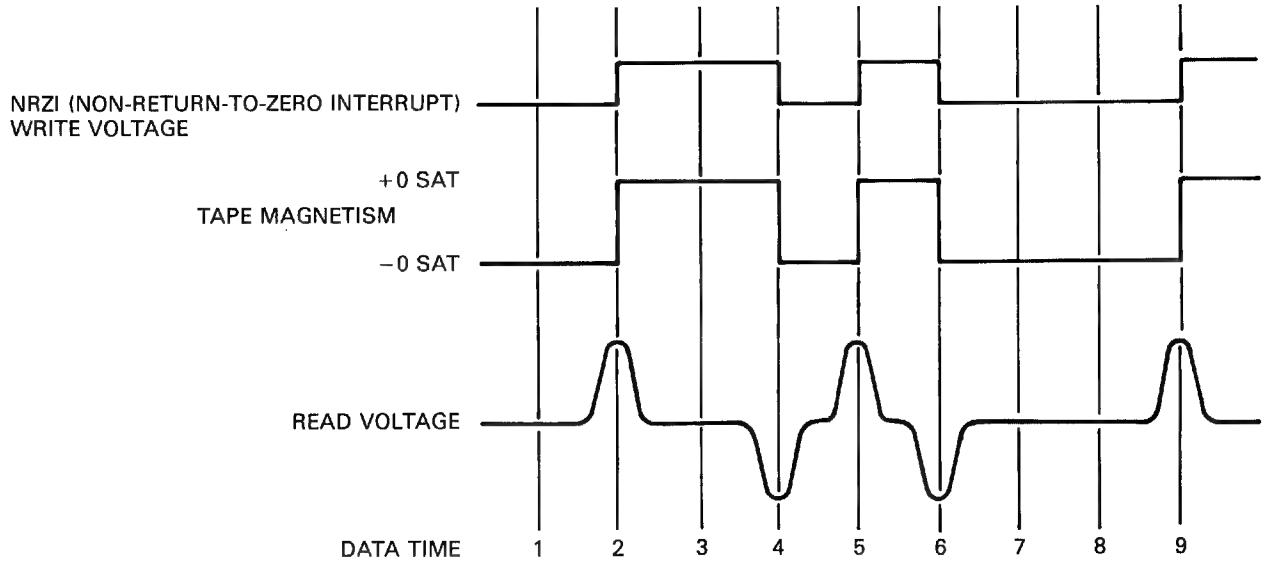


Figure 2-1. NRZI Recording Waveforms

Group Coding Process. In the group coding process, every four bits of data along each of the nine tracks are translated into a five-bit code that is recorded to tape. When it is read back, the translation is reversed and the actual data values are derived by the read logic. Since there are twice as many five-bit combinations as there are four-bit possibilities, five bit codes are selected to ensure that no code will contain more than two consecutive zeros, and that a run length of more than two consecutive zeros cannot occur no matter how the codes are linked.

The four-bit data values and the corresponding five-bit GCR codes are shown in Table 1. The GCR conversion and storage process is shown in Table 2. The data structure prior to GCR coding is shown in the DATA SUBGROUPS column; the translated five-bit codings are shown in the STORAGE SUBGROUPS column.

The levels of redundancy used in the GCR process to ensure data integrity include:

- Serial checks by track in five-bit segments

- Parallel checks of each translated data character using vertical parity

- Cyclic checks of each seven characters using the Error Correction Code (ECC).

GCR Format

Details of the GCR format are shown in Figure 2-2.

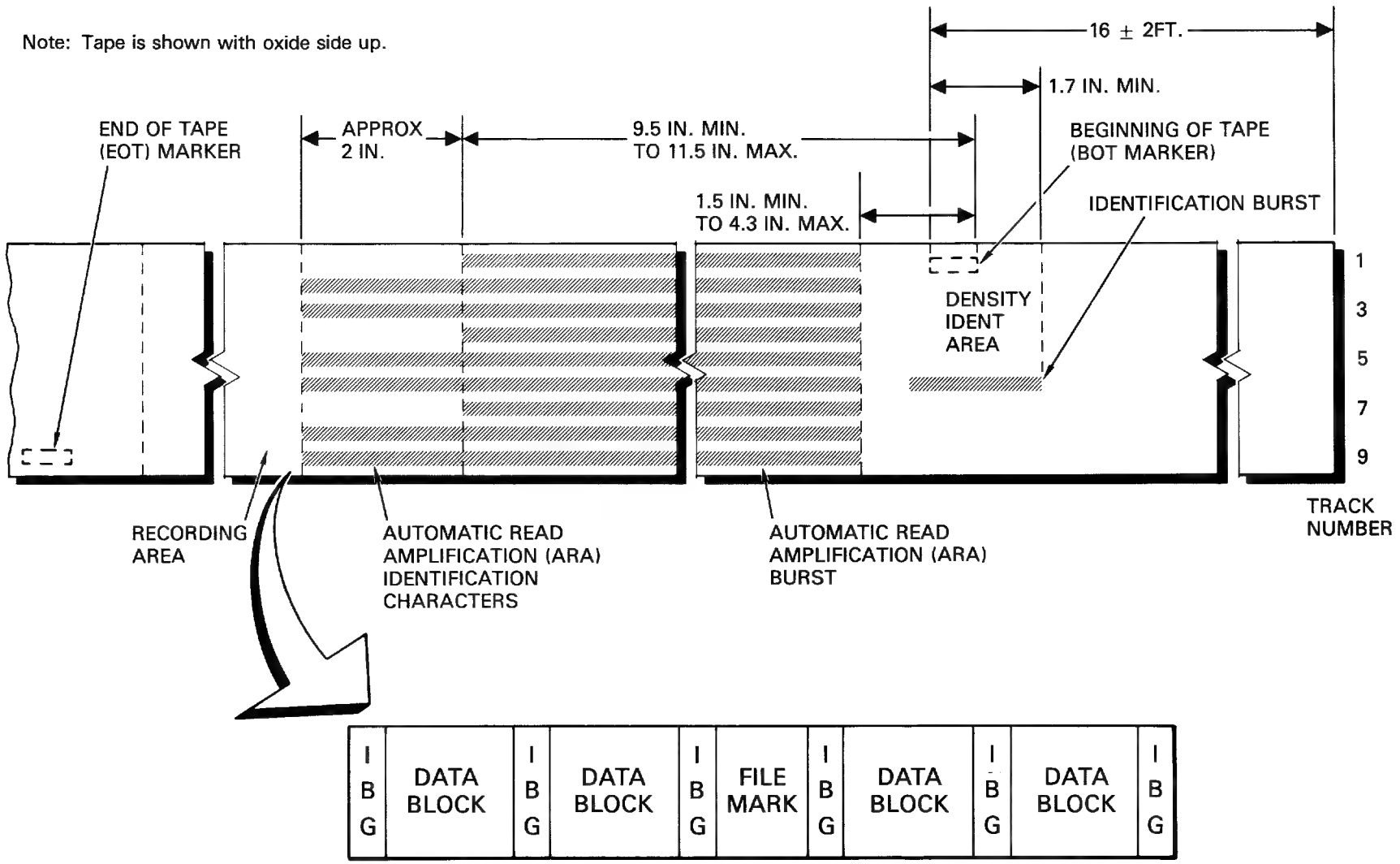


Figure 2-2. GCR Data Format

The GCR recording method is identified by and Identification (ID) burst in conjunction with the Beginning-of-Tape (BOT) marker. The burst is in the PE frequency range on track 6, with erasure on all other tracks. The burst must begin at least 1.7 inches ahead of the trailing edge of the BOT marker and extend beyond the trailing edge of the marker.

Following the ID burst is an Automatic Read Amp (ARA) burst of all ones in all tracks, separated from the ID burst by an unspecified gap. The ARA burst begins no sooner than 1.5 inches and no later than 4.3 inches from the leading edge of the BOT marker. It ends no sooner than 9.5 inches and no later than 11.5 inches from the leading edge of the BOT marker. Appended to the end of the ARA burst is an ARA identification character consisting of ones in tracks 2, 3, 5, 6, 8, and 9 and erasure in tracks 1, 4, and 7. The ARA ID character is approximately 2 inches long.

There is normal Interblock Gap (IBG) between the ARA ID character and the first data block. The IBG is nominally 0.3 inch long, with a minimum length of .28 inches and a maximum length of 15 feet. The IBG is used to separate blocks of information on the tape.

The GCR file mark is a special block written only by a Write File Mark command. The file mark consists of 250 to 400 flux reversals in tracks 1, 2, 4, 5, 7, and 8 with no recording in tracks 3, 6, and 9. The file mark indicates the end of a file of information.

A data block consists of a group of contiguous characters that are transported as a block. The data blocks are separated by interblock gaps. The end of a block is flagged by appending the Interface Last Word (ILWD) control signal to the last character of the data block. While the ANSI specification defines a data block as a minimum of 18 characters and a maximum of 2048 characters, there are no technical restrictions in the GCR recording technique to limit a data block to that size, and the specification permits relaxation of the size requirement upon agreement of the interchange parties.

Each data block includes a preamble and postamble, each consisting of 80 characters. The first five characters of the preamble are 10101, the second five characters are 01111, and the remaining 70 characters are 11111 in all tracks. The postamble is a mirror image of preamble, consisting of 70 characters of 11111, five characters of 01111, and five characters of 10101, in which 1 is the last character control signal.

The preamble is followed by a Mark 1 control subgroup, which consists of nine parallel five-bit serial values, 00111 in the respective tracks. The Mark 1 control subgroup is followed by the data, which is then followed by an end mark consisting of nine parallel five-bit serial values, 11111 in the respective tracks.

The end mark is followed by the residual and CRC groups. The actual number of data groups can be calculated by dividing the number of data characters by seven. Any remainder is accommodated in the residual group. The residual group also contains an auxiliary CRC character that is used for error detection and correction. An ECC character is also calculated for the residual group.

The CRC group consists of a CRC character written five or six times, depending upon the number of data groups in the data block. If there is an even number of data groups in the data block, a pad character is inserted as the first character in the CRC group. If there is an odd number of data groups of data groups in the data block, the CRC character is written in this location. This ensures odd parity for the CRC character.

The Mark 2 control subgroup follows the CRC group. This subgroup consists of one set of nine parallel five-bit serial values, 11100 in the respective tracks. This followed by the postamble, which ends with the last character control signal.

A resync burst is interleaved in the block every 158 data groups. This burst consists of one Mark 2 control subgroup, two synch subgroups, an a Mark 1 control subgroup. The resync bursts are used to resynchronize the operation of the read circuits when the bursts are sensed.

2.3 PHASE-ENCODED (PE) RECORDING

Phase-encoded (PE) recording is used for 1600 bits per inch (BPI) format in the nine-track mode only. The PE technique is illustrated in Figure 2-3. A major advantage offered by the PE format is the fact that the data is self clocking which allows each channel to be synchronized using a preamble.

a. There must be a change of tape polarity between data bits of the same polarity (consecutive 1 or 0 bits) at a time.

b. There must be a change of tape polarity at each data bit time.

c. There must not be change of tape polarity at phase time between 1 and 0 bits.

d. A change of tape polarity at data bit time, when reading forward; to erase polarity is a 1, away from erase polarity is a 0.

e. The PE transport records and reads data at a density of 1600 bits per inch (BPI).

For clarification, the term "change of polarity" is also referred to as a flux change or flux reversal. As noted above, there must be a flux reversal with each data bit, whether it be a 0 or 1. Therefore, 1600 BPI equates to minimum of 1600 flux reversals per inch (FRPI) in any given channel. (This would occur in the case of alternate 0 and 1 bits.) The maximum case would occur with consecutive 0 or 1 bits, resulting in 3200 FRPI. The flux reversal at each bit time accounts for the self-clocking feature of PE writing.

Details of the PE format are given in Figure 2-4. Channels 0 through 7 contain data bits, with the bit in channel 0 as the most significant bit. Channel P contains the parity bit, which in the PE format is always odd. No Cyclic Redundancy Characters (CRC) or Longitudinal Redundancy Characters (LRC) are used in the PE format. Each PE data block, however, is preceded by a preamble consisting of 40 bytes of all zeros followed by one byte of all ones. This is used to establish synchronization for the data block. The all-ones byte identifies the end of the preamble and the start of the data bytes in the block. Following each PE data block is a postamble which is the mirror image of the preamble; i.e., one byte of all ones and 40 bytes of all zeros.

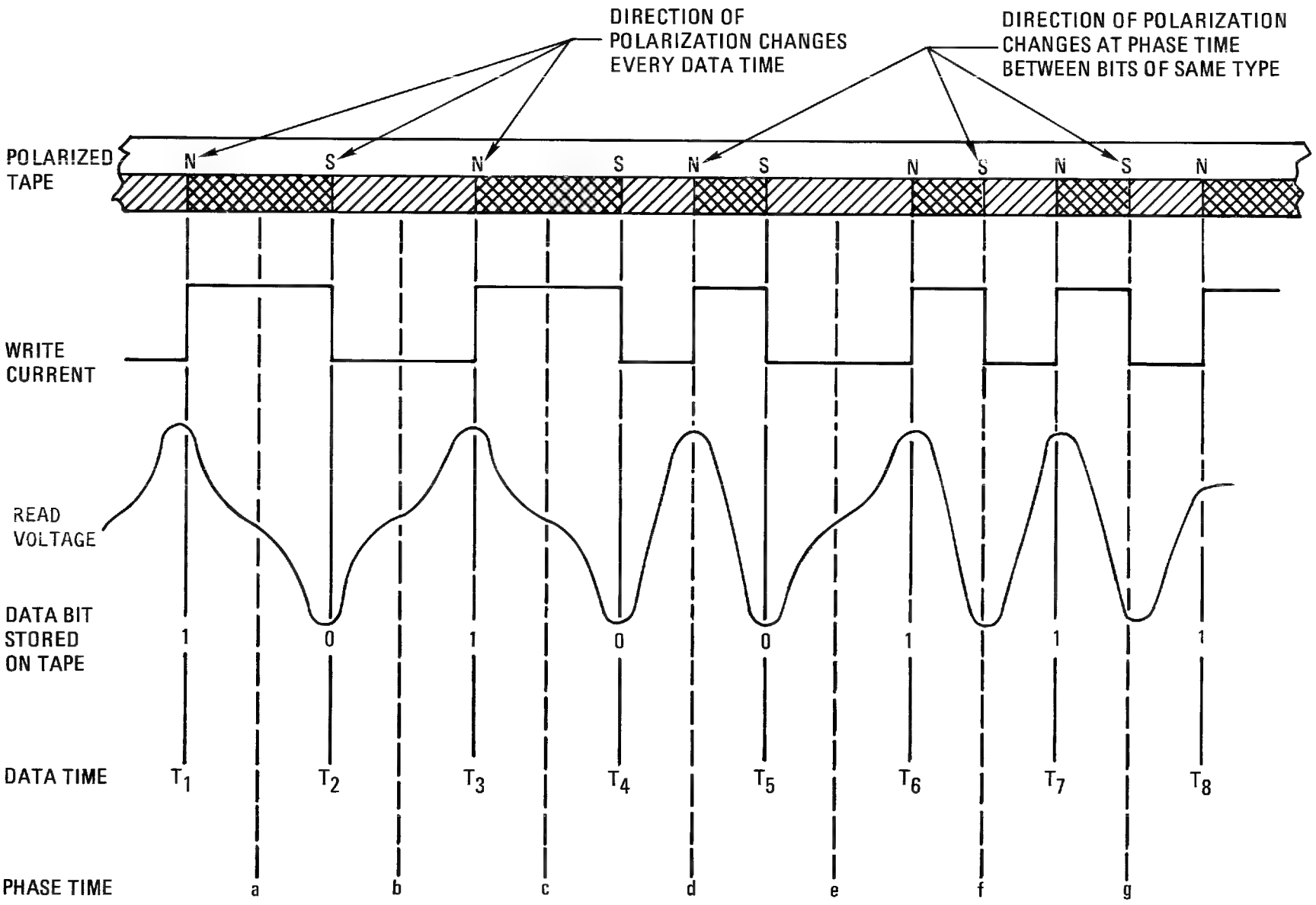


Figure 2-3. Phase-Encoded (PE) Tape Magnetization

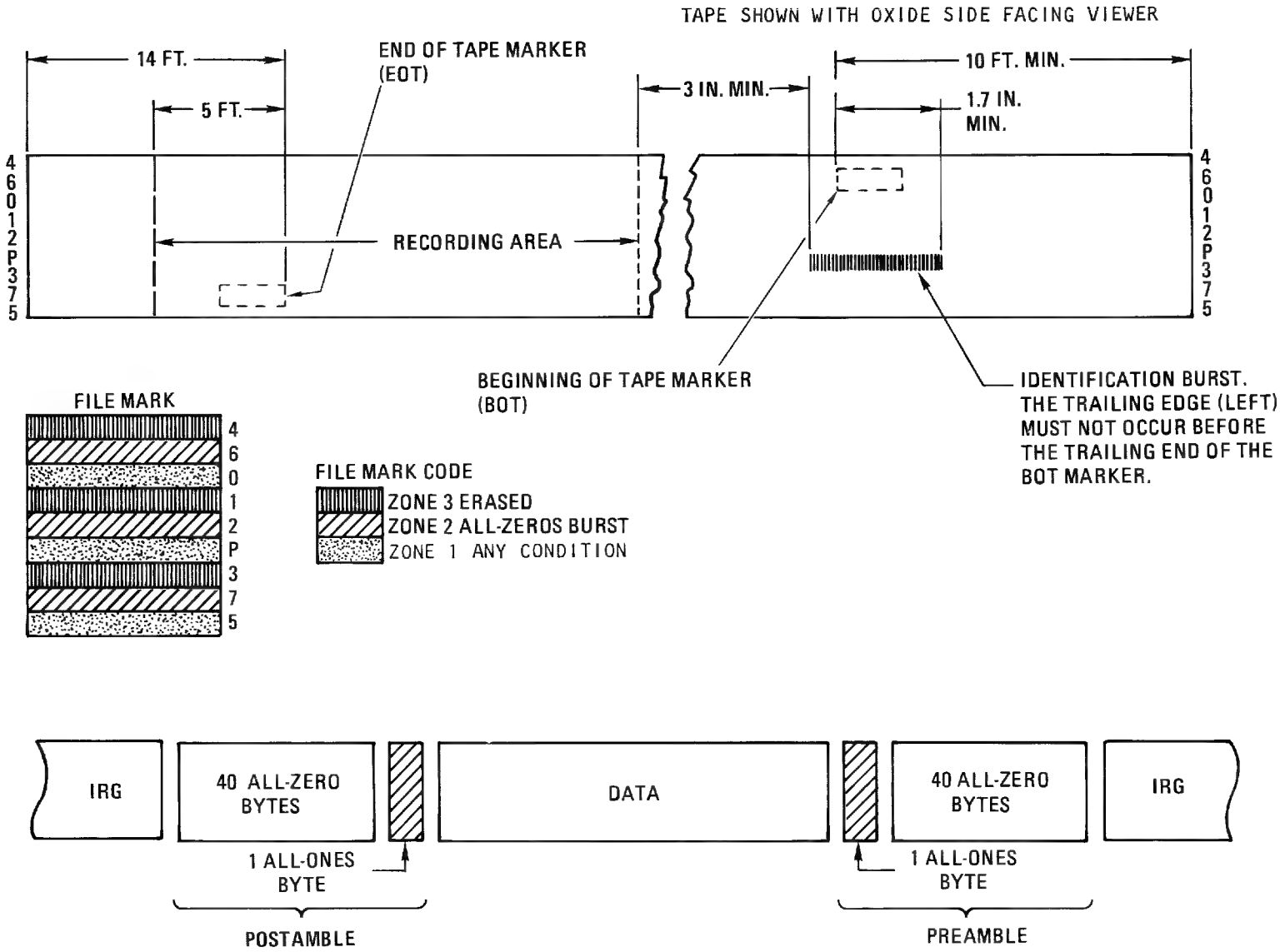


Figure 2-4. Nine-Track PE Data Format

A 1600 BPI phase-encoded tape requires an identification burst (ID) of 1600 FRPI in the P channel and erasure in all other channels at the beginning of the tape. The burst must begin at least 1.7 inches ahead of the trailing edge of the beginning of tape (BOT) marker and extend beyond the trailing edge of the marker and end at least 0.5 inch before the first block of data. The initial gap requirements are given in Figure 2-4. The typical distance for a gap is 3.75 inches.

The ANSI specification defines a PE file mark as a special control block consisting of 64 to 256 flux reversals (at 3200 FRPI) in channels 2, 6, and 7. Channels 1, 3, and 4 are dc erased, but channels, O, P, and 5 in any combination, may be dc erased or recorded in the manner stated for channels 2, 6, and 7. The GCR writes and IBM compatible file mark with 80 flux reversals (40 characters) at 3200 FRPI in channels P, O, 2, 5 ,6, and 7 with channels 1, 3, and 4 dc erased. The PE file mark is preceded by a gap of approximately 3.56 inches followed by a normal interblock gap (IBG) of 0.6 inch.

2.4 CACHETAPE OPERATION

CacheTape operation consists of the GCR receiving data from the host computer, placing the data in cache memory, and then writing the data on tape when the physical write head is available. This permits faster write speeds, when viewed from the host system, in that write data, as it is available, is transferred to the CacheTape* unit and stored in cache memory. The GCR then writes the data on tape in a time frame independent of the host transfer rate. The cache memory allows the GCR to perform most of the housekeeping chores normally assigned to the host, freeing the host for other system activities. The cache memory thus acts as a logical drive in its interfacing with the host.

The cache memory has storage limits that are reduced as the amount of tape remaining on the supply reel approaches end-of-tape (EOT). The system determines an impending EOT detection approximately ten feet in advance of the EOT marker and lowers the cache limits accordingly to assure that all data contained in cache will be written on the tape. The system operates in a streaming mode, as described below. When the cache is full and no further write data can be accepted from the host, Data Busy Line to Host will be held high until the cache is depleted below the selected block limits.

2.5 STREAMING-TAPE OPERATION

Streaming tape operation is simply writing data to tape without stopping and starting between each record block. Interblock gaps, as required in the ANSI format, are inserted automatically "on the fly". Figure 2-5 illustrates in the simplest form what a streaming drive will automatically perform if for any reason the unit must start and stop after each block. As can be seen in the diagram, there is a period of time called Command Reinstruct Time. This is the time after reading or writing the last character of the last block in which the microprocessor system must instruct the tape drive to continue or, after reaching point B, the tape drive will enter what is called repositioning cycle. If the command to continue reading or writing is not received by the time normal forward velocity reaches point B, the drive automatically decelerates, coming to rest at point C. Accelerates in the opposite direction, begins to decelerate, after coming to rest at point E, the unit waits for the next command to read or write. This sequence is called repositioning.

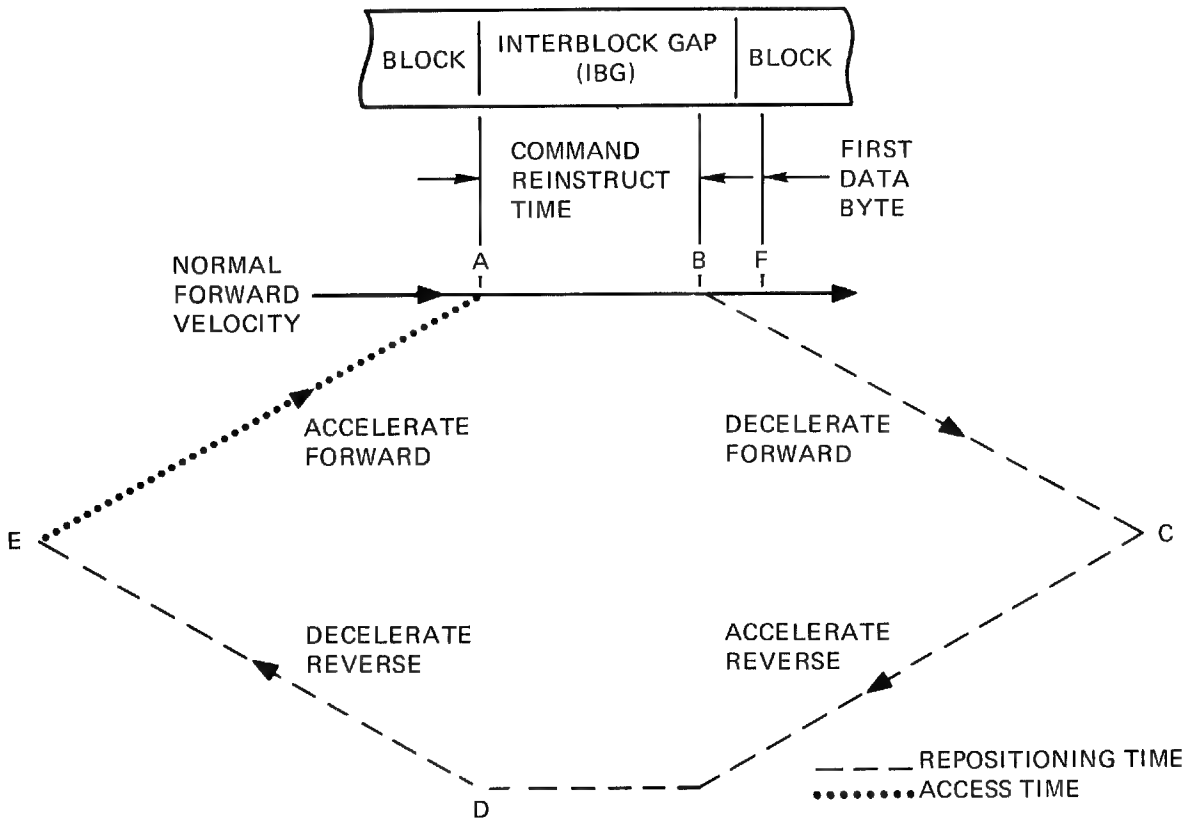


Figure 2-5. Repositioning Cycle

Because the tape acceleration and deceleration times required by the GCR are not related to tape velocity by the usual formula, it is not possible to start and stop the tape in the normal interblock gap (IBG). It therefore becomes necessary, during certain command sequences, to reposition the tape so that it will be in the correct position with respect to the record head when record velocity is attained following a subsequent command. However, if the subsequent command is of the same category and is given within the reinstruct time, repositioning will not be required; tape motion will continue at the normal recording velocity.

Repositioning. Repositioning is accomplished in three steps:

a. Deceleration of tape to rest position (forward).

b. Acceleration of tape to a maximum velocity in the opposite direction.

c. Deceleration of tape to rest position (reverse).

Figure 2-6 illustrates these three steps and shows the relative positions of the record head with respect to the recorded data. The velocity achieved during acceleration is equal to the record velocity of the tape. A write operation is used for the purpose of illustration: however, a read operation is identical, except that recorded data might be on either side of the record head. Figures 2-6A, B, and C show the position of the head and the last data block following acceleration or deceleration. Figure 2-6D is a composite showing the position of the record head at any instant in time during

repositioning. Segments AB, BC, and CD represent the actual repositioning, and segment DA is the acceleration after another command is issued (access time).

To allow for minor variations in acceleration and deceleration rates, the tape is allowed to run at speed for short distances during repositioning. This provides an offset, which is shown as points C and C' in Figure 2-6D. After repostioning, the record head might be left several data blocks in front of the point at which the next write or read operation is to take place. If one microprocessor command is followed by another in the opposite direction, it becomes necessary to perform an additional repositioning to allow the required distance for tape acceleration, as illustrated in Figure 2-7. This illustration represents a reverse read following a write forward. It can be seen that the second reposition is a retrace of the first. It is shown offset in time for clarity only.

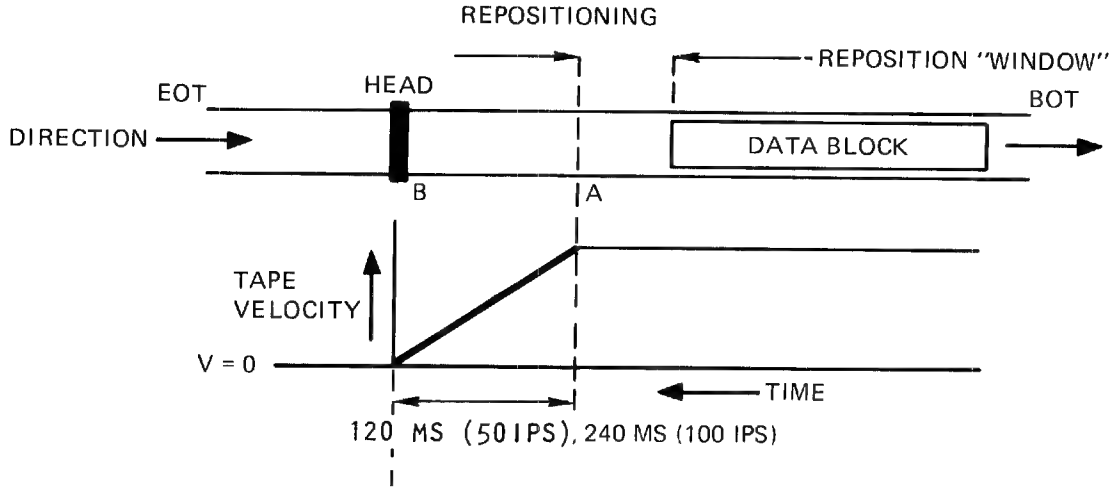


Figure 2-6A. Ramp Down (FWD)

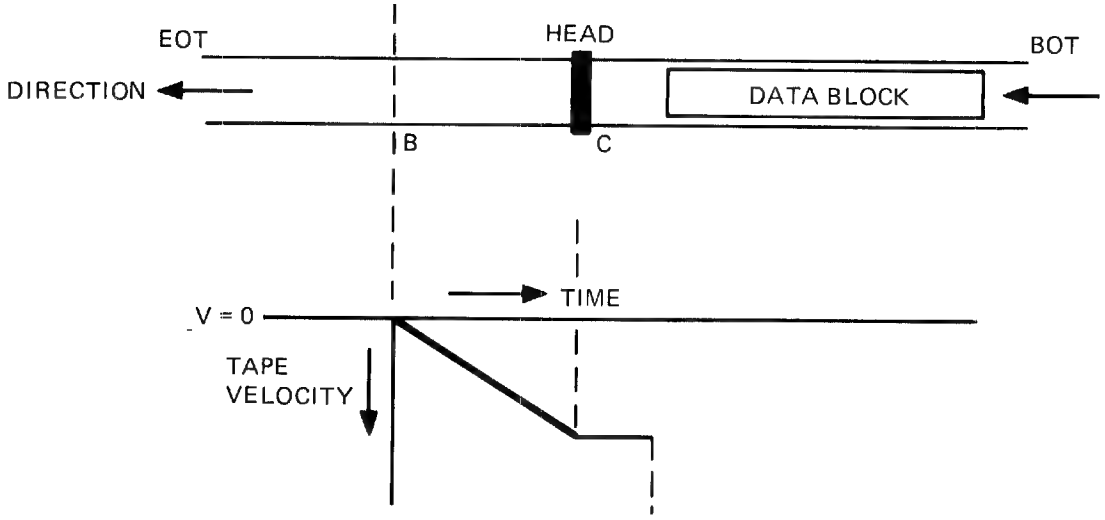


Figure 2-6B. Ramp Up (REV)

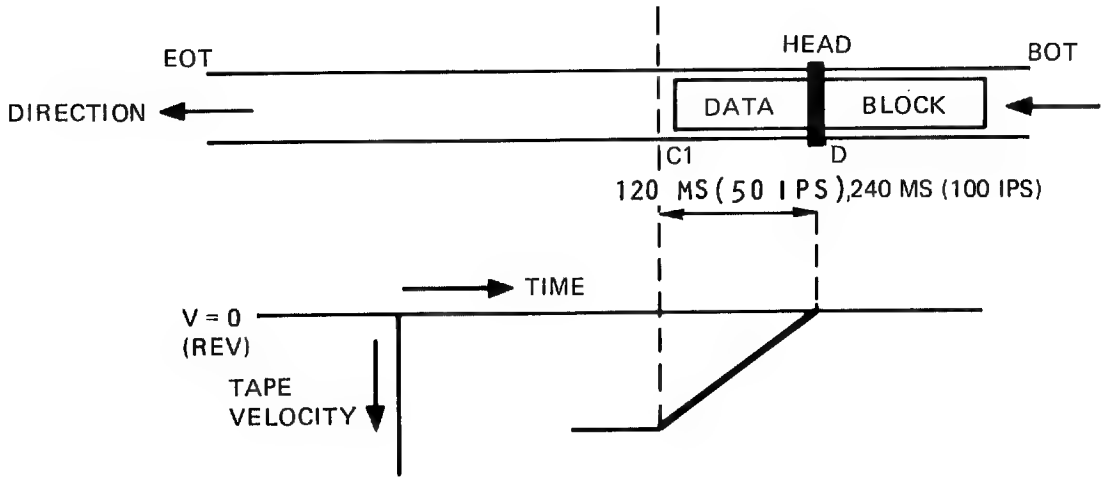


Figure 2.6C. Ramp Down (REV)

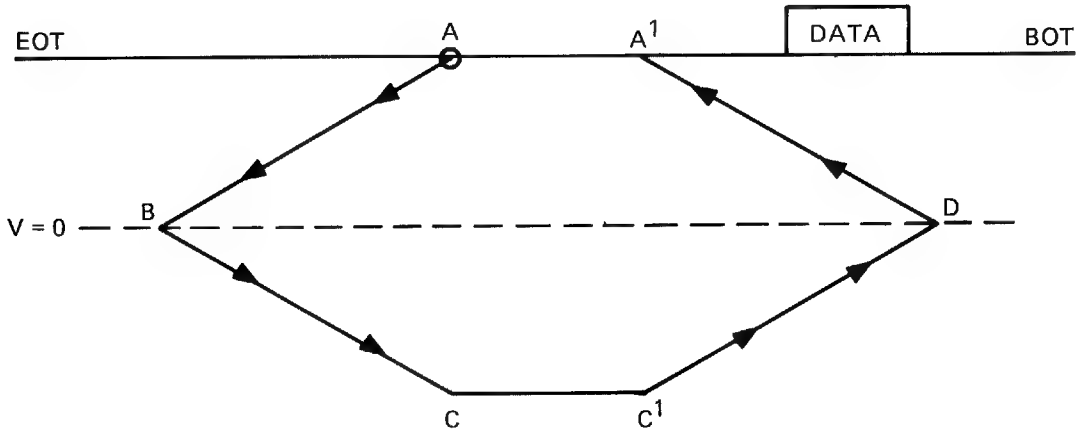


Figure 2-6D. Composite Ramps at 100 IPS.

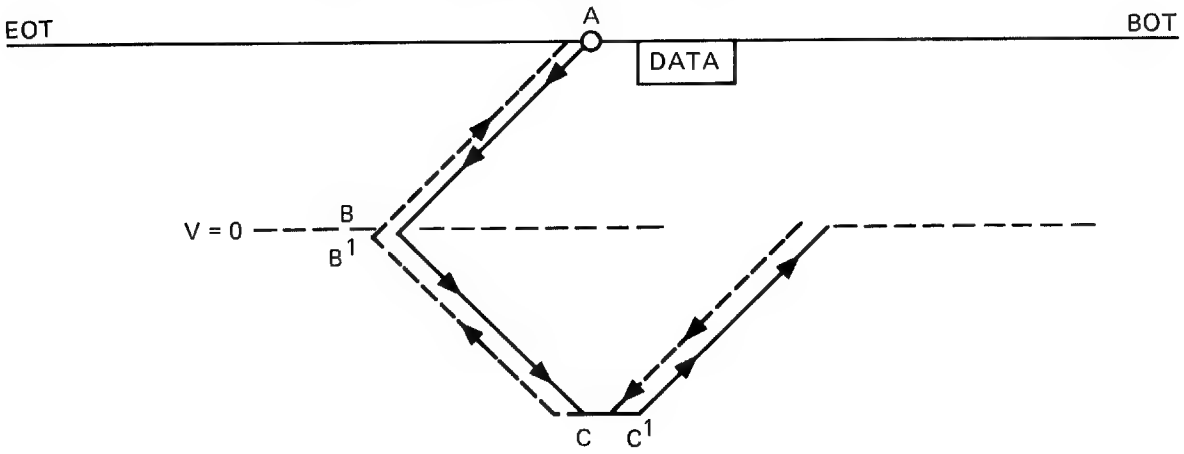


Figure 2-7. Reverse Direction Repositioning

DETAILED CIRCUIT DESCRIPTIONS

CHAPTER 3.

3.1 SENSE/SERVO BOARD (PWB 961344-XXX)

The Sense/Servo Board is a multiple-function PWB that contains the following circuits:

- o Voltage sourcing and regulation
- o Sensor signal processing
- o Mechanical actuations/drivers
- o Erase/Write Head drive
- o Compliance arm position sensing
- o Analog-to-Digital Converter
- o Supply reel servo driver
- o Take-up reel servo driver
- o Operator Panel interface
- o Alphanumeric Display Panel interface
- o Communication control

All top plate connections, except for data to and from the head, are made through the Sense Servo Board. The board provides voltage for all other system boards, and all direct external communications are made through the board via the Operator Control Panel, Alphanumeric Display Panel, or Serial Interface.

The following detailed descriptions of the Sense/Servo Board functions are based on Schematic No. 1. All sheet number references in the description refer to sheet numbers of that figure.

Voltage Sourcing and Regulation (See Sheet 2)

Voltage sourcing and regulation is performed on the Sense/Servo Board. Unregulated input voltages are received from Power Supply Module PS1 and via connector J1. A 3524A integrated circuit (U3V) is used to achieve switching regulation. The switching frequency of 25 kHz is determined by resistor R81 and capacitor C52. The 3524A drives a push-pull power stage consisting of transistors Q3, Q4, Q7, and Q8, which actuate current boost transformer T1.

Voltage regulation is taken from the secondary of the transformer T1 5-volt tap after frequency filtering through inductor L4 and capacitor C13. The +5-volt transformer output is rectified and sent to all system logic via connector P4.

Monitoring of the unregulated 57V dc input is done through comparator U3T. If the input drops below 38V dc, U3T will shut down the switching regulator U3V. In addition, one-shot U4V will send a power-on reset signal (PWR RES) to the microprocessor when power is applied.

Sensor Signal Processing (See Sheet 3)

The sensor input signals are received at J7 and J8, and consist of the following:

- o Take-up reel tachometer
- o Door sensor
- o File protect sensor
- o Beginning-of-tape (BOT) sensor
- o End-of-tape (EOT) sensor
- o Tape-in-path sensor

The sensor input signals are detected, shaped, and processed through comparators U10L and U11L. The resulting TTL-compatible signals, with the exception of the tachometer outputs, are fed directly to CIO U12B, (Sheet 7) for processing by the microprocessor. The tachometer outputs (TP0 and TP1) are pulse-shaped and conditioned by U17E and U17H (Sheet 7) before being routed to the CIO.

Mechanical Actuators/Drivers (See Sheet 3)

The following functions are controlled by the Sense/Servo Board:

- o Blower motor
- o Door lock solenoid
- o Hub lock solenoid

The Blower (BLWR), Door Lock (DRLK), and Hub Lock (HBLK) signals are sent from the microprocessor via CIO U10B (Sheet 7). The BLWR signal controls the blower motor through transistor Q1; the DRLK signal controls the door lock solenoid through driver U9G-10 and transistor Q13; and the HBLK signal controls the hub lock solenoid through driver U9G-8 and transistor Q13.

Erase/Write Head Drive Circuits (See Sheet 3)

The system uses three separate magnetic head assemblies; the erase head, the early erase head, and the write head. The drive circuits for these heads are located on the Sense/Servo Board. The drive circuits are controlled by signals from the microprocessor sent via CIO U10B (Sheet 7). The Erase Head 1 Enable (EH1EN) signal controls the operation of the erase head drive circuitry, which consists of driver U9E-2, transistor Q10, and related discrete components. The Write Enable (WEN) and 6250 signal control the operation of the write center tape head drive circuitry, which consists of drivers U9E-6, U16J-12, and U9E-4; transistors Q11 and Q12; and related discrete components.

Compliance Arm Position Sensing (See Sheet 3)

Signals indicating the position and rate of change of position of the compliance arm are generated by the compliance arm sensing logic. The compliance arm drive signal is derived from the 40 kHz SERVCLK output of CIO U10B-19 (Sheet 7) by drivers U16J-4 and -6; operational amplifiers U17K-10 and U15K-4; and related discrete components. A variable capacitor couples the compliance arm sense signal (ARMSNS) to U15K-1, where the arm position (ARMPOS) signal is generated by U15K-3 and related discrete components. The ARMPOS signal is routed to the Analog-to-Digital Converter (Sheet 4) via multiplexer U5E. The ARMPOS signal is also applied to differentiation circuit at U15K-12, consisting of U15K-14, U15K-10, and related discrete components. The output at U15K-10, Arm Division (ARMDIV), is also sent to the Analog-to-Digital

Converter (Sheet 4) via multiplexer U5E to indicate the rate of change of the position of the compliance arm.

Analog-to-Digital Converter (See Sheet 4)

The Analog-to-Digital Converter (ADC) provides communications between various analog signals and the microprocessor. The ADC consists of ADC1001 (U7D) and two 4051 multiplexers (U4E and U5E). The following analog lines are multiplexed and digitized for transmission to the microprocessor:

- o +12V
- o -12V
- o +5V
- o +57V
- o Write Center Tap Voltage (WCTV)
- o Take-up Motor Voltage/Current (TMV/TMI)
- o Supply Motor Voltage/Current (SMV/SMI)
- o Arm Division (ARMDIV)
- o Arm Position (ARMPOS)

The active multiplexer U4E or U5E) is selected by the MDAC A/B signal from CIO U10B-28 (Sheet 7). The signal to be sampled is selected by the A, B, C address signals from CIO U10B-32, -31, and -30. The selected signal, after digitizing by U7D, is routed to the microprocessor on the higher order byte of the processor address/data bus (AD8-AD15).

Digital-to-Analog Converter (See Sheet 4)

The Digital-to-Analog Converter (DAC) provides communication between the microprocessor bus and various analog signals. The DAC consists of DAC 1006 (U7B), a 4051 demultiplexer (U7G), differential amplifiers (U6C-1 and U6C-7), voltage followers (U6D, U6E, and U6F), and related discrete components. The following analog functions are generated by the DAC:

- o Supply Motor Current (ISU)
- o Take-up Motor Current (ITU)
- o Read Amplifier Voltage Threshold (ITHR)

The DAC 1006 (U7B) receives bits AD6 and AD7 and the high order byte (AD8-AD15) of the processor address/data bus. The analog output is available at U6C-7, and is sent to demultiplexer U7G for selection. The demultiplexer is enabled by the MDAC signal from CIO U10B-33 (Sheet 7), and the output signal of the demultiplexer is selected by the A, B, C address signals from U10B-30, -31, and -32. The selected demultiplexer output signal is clamped by one of the high impedance voltage followers (U6D or U6E). The selected output charges the associated capacitor (C26 through C28 and C30) to the desired value, and since the demultiplexer output returns to a very high impedance state, the capacitor retains that value until the next refresh time. The output at U7G-12 is used as a calibration feedback signal to the DAC output.

Supply Reel Servo Driver (See Sheet 5)

The ISU signal from the DAC (Sheet 4) is the drive signal (supply current) for the supply reel servo driver. The ISU signal is applied via R278 to U14P where it is filtered. The signal is then modulated by a 20 kHz sawtooth (f+ and f-) at comparators U14T. The

sawtooth is generated by U15J and U14S from a 40 kHz Servo Clock (SERVCLK) signal initiated by CIO U10B-19 (Sheet 7). The pulse-width-modulated signals from U14T-1 and U14T-2 are applied to the gating network of U14V. If the ISU signal was negative, specifying forward reel movement, the signals from U14V-6 and U14V-8 are sent to driver transistors Q26 and Q27. The ISU was low, specifying reverse reel movement, the phase difference will result in reverse motion. The driver transistors feed an H-bridge power driver comprised of transistors Q18, Q19, Q22, Q23, and their related components, which drive the supply motor through inductors L5 and L6 and motor breaking relay K1. Voltage feedback is provided by comparator U9N-3, which generates the Servo Motor Voltage (SMV) signal that is sent to the Analog-to-Digital Converter (Sheet 4) for digitizing and routing to the microprocessor. Current feedback is provided by U9N-4, which generates Servo Motor Current (SMI) for routing to the microprocessor via the Analog-to-Digital Converter.

Current limit protection is provided by comparator network U14M. When the servo motor current exceeds its maximum limit, the High Current (HII) signal at U17J-4 goes low. This inhibits the U14V gating network, causing the servo drive to shut down (Sheet 6).

Further shutdown protection is provided by the Watchdog Timer logic (Sheet 6). If the +5V drops too low, the Servo Enable 2 (SERV EN 2) signal at U15H-8 goes low, inhibiting gate U17G (Sheet 5). This shuts off transistor Q2, deenergizing relay K1 and shutting down the servo drive.

Take-up Reel Servo Driver (See Sheet 6)

The operation of the take-up reel servo driver is similar to that of the supply reel servo driver. The ITU signal from the DAC (Sheet 4) is the drive signal (supply current) for the take-up reel servo driver. The ITU signal is applied via R280 to U14P where it is filtered. The signal is then modulated by the 20 kHz sawtooth (f+ and f-) from the supply reel servo driver logic at comparators U14T. The pulse-modulated signals from U14T-13 and U14T-14 are applied to the gating network of U12N. If the ITU signal was negative, specifying forward reel movement, the signals from U12N-6 and U12N-8 are sent to driver transistors Q25 and Q24; the phase difference will result in forward motion. The driver transistors feed an H-bridge power driver comprised of transistors Q16, Q17, Q20, Q21, and their related components, which drive the take-up motor through inductors L7 and L8 and motor breaking relay K1. Voltage feedback is provided by comparator U9N-12, which generates the Take-up Motor Voltage (TMV) signal that is sent to the Analog-to-Digital Converter (Sheet 4) for digitizing and routing to the microprocessor. Current feedback is provided by comparator U9N-10, which generates Take-up Motor Current (TMI) for routing to the microprocessor via the Analog-to-Digital Converter.

Current limit protection is provided by comparator network U14N. When the Take-up Motor Current exceeds its maximum limit, the High Current (HII) signal at U17J-4 goes low. This inhibits the U12N gating network, causing the take-up servo drive to shut down.

The take-up motor drive also has the further shutdown protection of the Watchdog Timer logic detailed in the description of the Supply Reel Servo Driver.

Operator Panel Interface (See Sheet 4)

The Sense/Servo Board processes control signals that operate a power switch, a power on indicator, and six tactile membrane switches with five associated light emitting diodes (LEDs) on the Operator Control Panel. The LEDs are controlled by the LOAD, UNLOAD, ON-LINE, WRT EN, and HI DEN signals from CIO U12B (Sheet 7) through drivers U12H. The switches are sensed by a resistor divider circuit and the same CIO lines that drive the LEDs.

Alphanumeric Display Panel Interface (See Sheet 7)

The Alphanumeric Display Panel contains an eight-character (ASCII) fourteen-segment display and three density display LED bars. When the alphanumeric display or LED display address is decoded by U15E (DSPSL or LEDSL, respectively), data is sent to the selected display via drivers U12G and U13G on the BAD0-BAD5 lines.

Communication Control (See Sheet 7)

Communications between the Sense/Servo Board and the microprocessor is accomplished by reading and writing to memory locations corresponding to six memory-mapped input/output devices. These devices are the two CIOs (U10B and U12B), the Analog-to-Digital Converter (U7D), the Digital-to-Analog Converter (U7B), and the density and alphanumeric displays located on the Alphanumeric Display Panel. Addresses within the Sense/Servo Board memory space are latched by U15B and decoded by U15E. After decoding, the active output of U15E enables the selected I/O device.

3.2 CPU/MMU BOARD (PWB 961730-XXX and 962112-XXX)

The CPU/MMU Board consists basically of three logic groups: the CPU and associated control and storage logic; the cache RAMs; and the control and management logic for the cache memory area. The logic groups perform the following functions:

- The CPU logic group consists primarily of the Z8002 microprocessor, the Z8036 counter and I/O (CIO); the microprocessor RAMs and PROMs; a NOVRAM; and associated control logic chips. The CPU logic group monitors and controls the physical and logical processes of the GCR.

- The cache RAMs provide a logical tape area for data that is to be written to the physical tape or that has been read from the physical tape. The cache RAMs thus act as a data buffer between the host processor system and the physical tape transport system.

- The control and management logic group, called the Memory Management Unit (MMU), consists of the 2900 bit slice DMA controller and associated control logic. The MMU provides access control and management of the cache RAMs.

Each of these basic logic groups is described in detail in the following paragraphs. Refer to Schematic No. 2.

CPU Logic Group

The microprocessor, which is a Z8002A chip (U25B, Sheet 2) is supported by two 64K-byte banks of dynamic RAM (DRAM), consisting of a high-byte bank and a low-byte bank, as listed in Table 3.

The low-byte bank of DRAMs is used to store instructions and special input/output operations. The high-byte bank is used to store stack data and to perform housekeeping operations.

The microprocessor is also supported by 64K bytes of EPROM (U20K, U23K, U22K, and U25K, Sheet 5). The EPROMs contain start-up data and are accessed only during boot-up following a power-up reset.

The microprocessor operates at two speeds. During boot-up, it operates at 2.7 MHz to allow program data to be read from the relatively slow EPROMs and written into the DRAMs. This is controlled by a clock conditioner (U27C). The clock conditioner divides the clock by two in response to the BOOT signal, which is high during boot-up. The BOOT signal is generated at U25D-11 (Sheet 3) by a Power Reset (PWRRES) signal. It is reset under software controlled by RBOOT from address decoder U27J (Sheet 7). During boot-up, the clock conditioner not only controls the width of the clock pulses to the microprocessor, but also provides the NMOS levels and 10-nanosecond rise and fall times necessary for proper microprocessor operations. At the conclusion of boot-up, the BOOT signal is turned off by the software, and the microprocessor is clocked at its full speed of 5.4 MHz.

The microprocessor communicates with the system via bidirectional address/data lines ZAD0-ZAD15. When the start cycle is initiated, the microprocessor sets up the address for that cycle on the address/data lines and issues the Address Strobe (AS) at U25B-29. The rising edge of AS indicates that the addresses are valid. The address strobe is routed to the enable input (pin 11) of address latches U22F and U27F via U27H-6 and U23B-6. The ZAD0-ZAD15 addresses are latched into the address latches on the trailing (rising) edge of AS.

Data line buffers U23F and U25F also receive addresses and data on the ZAD0-ZAD15 lines. The addresses and data are sent to other portions of the CPU/MMU board via buffered address/data lines BAD0-BAD15.

The microprocessor generates status signals (ST0-ST3) at U25B-21, -20, -19, and -18. These signals define the current processor status, and are sent to a decoder (U23C) to activate the specified status line. The status line output codes and the active decoder lines are listed in Table 4.

The REFRESH, IO, and SPECIAL IO status signals are used in the DRAM timing logic. SPECIAL IO is used during boot-up to prevent microprocessor reading or writing in instruction space other than instruction latch (Sheet 3). DATA + STACK, which is used by DRAM timing logic on Sheet 3 to generate Boot Read (BOOT RD). INTA is sent to the interrupt acknowledge input of CIO U20D (Sheet 7), and IO is used as an enabling input to address decoder U27J in the CPU/DMA interface logic (Sheet 7). Both IO and INTA are routed to other boards via buffer U22A and processor bus connector J5 (Sheet 6). The DATA + STACK signal is also used (Sheet 2) to generate the HBANK signal, which when active, selects the high DRAM bank. DATA + STACK is applied to Exclusive-OR gate U18J, and when REVERSE BANKS from the CPU/DMA CIO (Sheet 7) is high, HBANK is also high. HBANK is sent to the address multiplexer (U18M, Sheet 5) to specify the high bank has been selected.

Logic in the DRAM timing circuits (Sheet 3) generates Row Address Strobe (RAS) and Column Address Strobe, High and Low (CASH and CASL) for the DRAMs. The RAS is generated by U20B-6 on the rising edge of ZCLK from the microprocessor clock logic (Sheet 2). The Address MUX (AMUX) strobe is set at U23D-8 (Sheet 3) to enable the

high order address (row address) from DRAM address/MUX buffer U18M (Sheet 5). The Memory Request (ZMREQ) signal from the microprocessor then toggles U23D (Sheet 3) via exclusive -OR gate U18J-13 on the next portion of the cycle, sending AMUX low to enable the low order address bits (column address) from DRAM address/MUX buffer U27M (Sheet 5). The Column Address Strobe High (CASH) and Low (CASL) are generated at U27P-18 and U27P-16 (Sheet 3) respectively. CASL, or both CASL and CASH, are generated, depending upon the state of latched address 0 (LA0) from the microprocessor address latches. The LA0 signal is used to address decoder U27D and specifies either byte or word mode. In the byte mode, CASL is generated; in the word mode, both CASH and CASL are generated.

During IO operations, ZIO from the microprocessor is high at gate U23H-2. Flip-flop U22B-8 is reset by ZCLK when RAS is generated, enabling U23H-1 and generating WAIT for one additional ZCLK period. This additional microprocessor wait state is actually required for off-card CIO access, but for logic simplicity it is used for all IO operations. Whenever a data byte is written into DRAM, a parity bit is generated by parity generators/checkers U23J and U22J (Sheet 4), and is also written into DRAM. Whenever a data byte is read from DRAM, the parity is checked by U23J and U22J. If a high- or low-byte parity is detected, or gate U20J-6 generates a Parity Error (PERROR) signal that sets flip-flop U20B-9, producing a low Watchdog Refresh Disable (WDOGR DIS) signal. This signal is sent to the CPU I/O buffers (U22A, Sheet 6), where it is routed to the Sense Servo Board via connector J5. During diagnostics, the FLMPE signal or the FHMPE signal from CIO U20D (Sheet 7) forces a parity error at U22J or at U23J, respectively (Sheet 4).

A 64 X 4 bit non-volatile RAM (U25J, Sheet 6), called a NOVRAM, is used to store GCR setup data. This data includes unit number, ramp speed, record block size, and interface transfer rates. The set-up data is mapped into the NOVRAM by the microprocessor, bit by bit, in an EEPROM memory array, from a static RAM memory. The set-up data represents the default initialization status of the GCR. A circuit consisting of transistors Q1 and Q2 and associated discrete components inhibits the NOVRAM store line to prevent false store and prevent store errors during power up.

Control and Management Logic Group

Control and management of the cache memory is provided by the Memory Management Unit (MMU). The MMU consists of a Direct Memory Access (DMA) controller and related logic that controls the interfacing of the microprocessor and the host interface with the cache RAMs (Sheet 7). Three access channels allow simultaneous loading and unloading of the memory. The counter/timer and parallel I/O unit (CIO U20D) interfaces with the microprocessor and provides control signals to the DMA controller. Two latches (U17K and U17L) route addresses from the microprocessor to the DMA controller. An address decoder (U27J) routes additional control signals from the microprocessor to the CPU control logic.

The MMU logic also contains the DMA Cache DRAM Control, which includes the counter/clock logic for the MMU; the Bit-Slice Processor Logic to provide cache memory addresses; and the RAS and CAS generation logic for cache DRAM location addressing and refresh.

DMA Control Logic. The DMA control logic (Sheet 7) provides the interface between the CPU and the DMA. The CPU and DMA operate asynchronously, with independent timing signals, on their respective sides of the interface logic.

The DMA control logic consists of a CIO (U20D), two address latches (U17K and U17L), and an address decoder (U27J). The CIO routes CPU control signals from the address/data lines (ZAD0 - ZAD7) to the DMA logic. The address latches route DMA address (DMA0 - DMA15) from the buffered address lines (BAD0 - BAD15) to the DMA cache DRAM control logic. The address decoder decodes four latched address lines (LA9, LA13, LA14, and LA15) from the CPU logic and activates one of six output control lines. The address decoder signals and their functions are listed in Table 5. The CIO control signals and their functions are listed in Table 6, and the CIO output signals and their functions are listed in Table 7.

DMA Cache DRAM Control

The DMA cache DRAM control logic consists of five interrelated circuits: the counter/clock logic; the channel clock generators; the bit-slice processor logic; the RAS0-3 generation logic; and the CAS0-3 generation logic. These circuits provide he following functions:

- Counter/Clock logic - Receives the 10.85-MHz DMA master clock from the CPU clock logic and divides this clock by two and four to produce the 5.43- and 2.71-MHz operation clocks for CAS/RAS generation, bit-slice processor timing, and channel clock generator timing.

- Channel clock generator - Produces three distinct clock phases (A, B, and C) that are used to clock three specific channels: Interface, CPU, and R/W.

- Bit-slice processor logic - Used to emulate a high speed three-channel DMA capable of addressing up to 256K bytes of memory.

- RAS and CAS generation logic - Generate the Row Address Strobes (RAS) and Column Address Strobes (CAS). RAS causes the row address locations of the cache DRAMs to be sensed; CAS causes the column address locations to be sensed. CAS controls the three-state output of the DRAMs, independent of RAS. RAS causes row refreshes to occur, independent of CAS.

Counter/Clock Logic. The counter/clock logic consists of counter U16F and clock decoder U16H (Sheet 8). Counter U16F receives the 10.85 UB DMA master clock signal from the CPU clock logic (Sheet 2), and divides the master clock by two and four to produce 5.43 MHz and 2.71-MHz clocks at U16F-3 and U16F-2, respectively. The 2.71-MHz, 5.43-MHz, and 10.85-MHz clocks are used by the CAS generation logic and the bit-slice processor logic. The 2.71-MHz clock is used by the channel clock generator (Sheet 9), and the 5.43-MHz clock is routed to the Data and CIF-Write boards via connector J3. The three clock signals, 2.71 MHz, 5.43 MHz, and 10.85 MHz, are all applied to clock decoder U16H (Sheet 8). The clock decoder produces negative-going timing pulses at U16H-15, U16H-13, and U16H-11 that are used by the bit slicer MUX logic and the RAS0-3 logic.

Channel Clock Generator. The channel clock generator (Sheet 9) consists of a ring counter (U16C-6, U16C-10, and U15C-6) and associated logic devices. The three ring counter flip-flops are clocked by the 2.71UB clock from counter U16F in the counter/clock logic (Sheet 8). With the three flip-flops in the reset state, the output at gate U14C-6 (Sheet 9) is high, causing the output of OR gate U17C to go high and setting U16C-6 on the first clock pulse. On the next clock pulse, U16C-6 is set. Similarly, U16C-10 is reset on the next clock pulse and U15C-6 is set. With U15C-6 set, the high at U17C-10 sends U17C-8 high, causing U16C-6 to again be set on the following clock pulse.

The three outputs from the ring counter (A, B, and C) are the INTERFACE CLK, CPU CLK, and R/W CLK respectively. These signals provide three distinct phases of cache operation: interface (phase A); CPU (phase B); and read/write (phase C). The clocks are routed to the CIF-Write and Data boards via connector J3-50, -52, and -54, respectively.

The clock signals also generate ABUF, BBUF, and CBUF (Sheet 9), which are used to address the DMA bit slice devices (Sheet 8).

Bit Slice Processor Logic

The bit slice processor logic consists of five bit slice devices, a bit slice multiplexer circuit, and associated logic. The bit slice devices generate the DMA addresses; the multiplexer circuit routes the addresses to the cache DRAMs.

Each bit slice device (U3K, U6K, U9K, U12K, and U14K, Sheet 8) has nine input control lines (I 0-I 8, as shown for U3K). However, only three lines (I 2, I 3, and I 4) are used in the GCR for microinstruction selection. The remaining six lines are held high or low to obtain the desired microinstructions as the three active lines are changed.

Three registers in the bit slice devices are used for DMA addressing. Each register is dedicated to a specific DMA address, and is accessed and manipulated during a specific clock phase (ABUF, BBUF, and CBUF). The register designators and their respective DMA addresses are listed in Table 8. The remaining bit slice registers are not used.

The functions performed by the registers during their respective clock phases are controlled by the microinstructions on the I 3 and I 2/4 lines and by the Carry In (CN) line. The input signals to the I 3, I 2/4, and CN lines are generated by data selector U18D (Sheet 9). The data selector receives the DOWN and LOAD signals for the IF, CPU, and R/W channels from the CIO (Sheet 7). The DOWN signals specify a count up or down command to the bit slice devices; the LOAD signals specify a load or run command. The data selector (Sheet 9) is addressed by two of the phase clocks, phase A and Phase C, to select the control signals for the IF, CPU, and R/W channels during the respective phase.

The two data selector outputs are applied to gates U17C and U14B. The I 2/4 output (U18D-7), when high, specifies a load operation, and sends I 3 high via OR-gate U17C-2. The data selector output at U18D-9, when high, specifies a count down, and sends I 3 high via U17C-1. When U18D-9 is low, and a load command is not present (I 2/4 low), I 3 is low, specifying a count up operation to the bit slice devices. Exclusive-OR gate U14B-3 generates a Carry In (CN) input to the bit slice devices when either U18D-9 is high or when the input to U14B-1 from the advance MUX (U17H-7) is high.

The advance MUX received WRITE ADV and INTERFACE ADV from the CIF Board and READ ADV from the Data Board via connector J3, pins 44, 42, and 43 respectively. When any of these signals is high during its respective channel time, the address counter in the bit slice devices will advance.

The bit slice devices receive the DMA addresses (DMA0-DMA17) from the CPU via address ports U17L and U17K (Sheet 7). The devices (Sheet 8) receive the microinstruction from the data selector on the I 3 and I 2/4 lines, and the Carry In (CN) signal from the data selector output XOR gate. The DMA addresses are loaded into the bit slice devices when the LOAD microinstruction is sent on the I 3 and I 2/4 lines.

Three operations are possible using the I 3, I 2/4, and CN lines. These functions are listed and described in Table 9.

The channel clock inputs (ABUF, BBUF, CBUF) to the bit slice devices select the appropriate registers (R1, R2, and R4) for incrementing/decrementing and for outputting via the Y outputs. During an ABUF (Interface) cycle, nothing is done with the corresponding address register (R1, LTAPE address). The bit slice devices output the R2 (CPU address) register via the Y outputs and increment or decrement the R4 (PTAPE address) register. Similarly, during a BBUF (CPU) cycle, nothing is done with the corresponding address register (R2), and during a CBUF (R/W) cycle, nothing is done with corresponding address register R4. The functions performed by the bit slice devices during the three channel clock cycles, and the associated microinstructions, are shown in Table 10.

The Y16 and Y17 outputs of bit slice device U14K are used in the CAS generation logic to select the CAS decoder output, as detailed in the CAS generation description. The Y0 - Y15 bit slice device outputs are sent to the bit slice MUX logic.

The bit slice MUX logic consists of MUX flip-flop U16K-5, latches U6J and U9J, and line drivers U3J and U12J. The MUX logic timing is shown in Figure 3-1. MUX flip-flop U16K-5 is clocked by the 10.85 UB clock and is initially set when the 5.43 UB clock is high. On the next 10.85UB clock pulse, the low U16H-15 pulse at the preset input

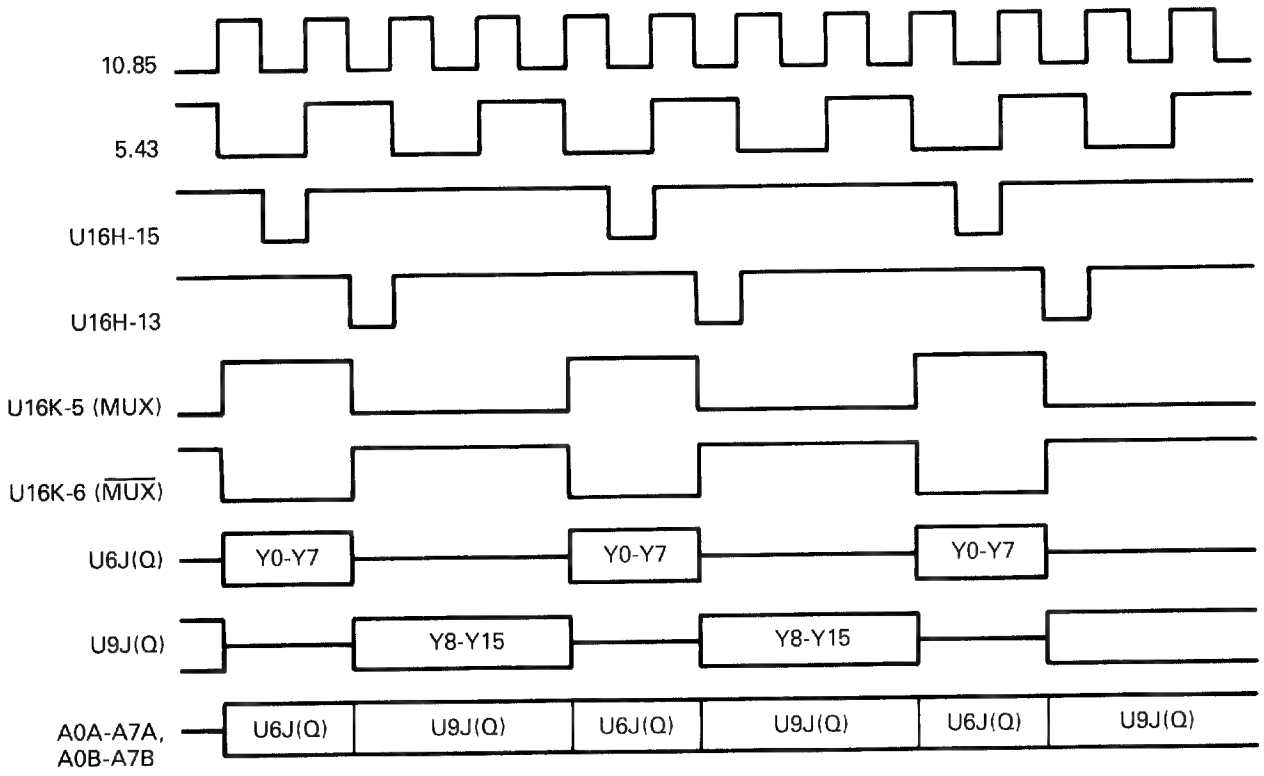


Figure 3-1. Bit Slicer MUX Logic Timing Diagram

(U16K-4) holds the MUX flip-flop in the set state. The flip-flop is reset when a low U16H-13 pulse occurs at the reset input (U16K-1). The positive-going edge of the U16K-6 (MUX) signal clocks the bit slicer output data (Y0-Y15) into latches U6J and U9J. The negative portion of the MUX signal enables the outputs of latches U9J. The negative U16K-5 (MUX) signal enables the outputs of latches U6J. The A0A-A7A and A0B-A7B outputs of drivers U3J and U12J, respectively, alternately route the U6J outputs (Y0-Y7) and the U9J outputs (Y8-Y15) to the cache DRAMs (Sheet 10).

The U16K output of the MUX flip-flop is also used to clock flip-flops U16L-5 and U16L-9 in the CAS generation logic.

RAS Generation, Write Enable, and Parity Check Clock Generation Logic (See Figure 3-2). The RAS generation logic consists of RAS flip-flop U15K-6, inverter U3C-8, and four drivers (U15F-12, -14, -16, and -18). The RAS flip-flop is set by the trailing (positive-going) edge of the U16H-11 pulse, sending U15K-5 high. This high is inverted by U3C-8, and the negative signal generates RAS0-RAS3 at the outputs of RAS drivers U15F-12, -14, -16, and -18. The RAS flip-flop is cleared by the leading (negative-going edge of the pulse.

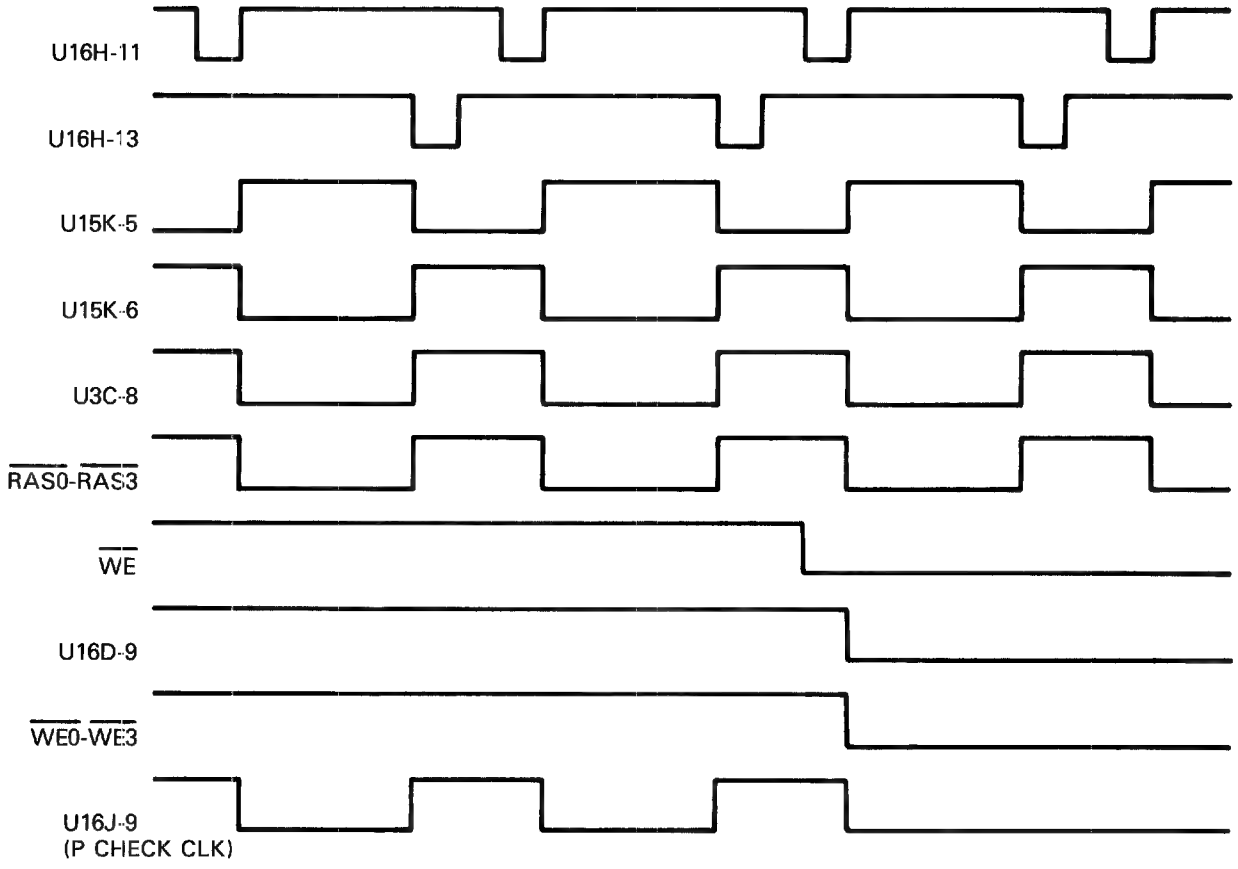


Figure 3-2. RAS Generation, Write Enable, and Parity Check Clock Generation Timing Diagram

The output of the RAS flip-flop at U15K-5 is used to clock flip-flops U15L-5 and U15L-9 in the CAS generation logic, and the Write Enable flip-flop (U16D-9). When Write Enable (WE) from the Read/Write (U18F-7) MUX (Sheet 9) is active (low), U16D-9 is reset on the next RAS flip-flop clock pulse. The low at U16D-9 (Sheet 8) generates WE0-WE3 via drivers U15F-3, -5, -7, and -9. The WE0-WE3 signals are used to enable to write function in the cache DRAMs (Sheet 10).

The outputs of the RAS flip-flop (Sheet 8) are also used to operate the Parity Check Clock (P CHECK CLK) flip-flop (U16J-9). The P CHECK CLK flip-flop is toggled by the U15K-5, and U15K-6 outputs to produce the P CHECK CLK signal when the output of Write Enable flip-flop U16D-9 is high. When U16D-9 is low, the P CHECK CLK flip-flop is held in the reset state and P CHECK CLK is not generated.

CAS Generation Logic. (See Figure 3-3). The CAS generation logic consists of CAS flip-flop U16J, gates U15H-3, -6, -8, and -11, and the CAS decoding circuit comprised of latches U16L and U15L, and decoder U14J. The CAS flip-flop is clocked by the 10.85UB clock signal, and is toggled by the 2.71UB pulse. The 2.71UB pulses are applied directly to U16J-3, and are inverted by U17J-12 and applied to U16J-2. The CAS flip-flop is thus toggled on the trailing edge of the 10.85UB clock following each transition of the 2.71UB signal. The CAS flip-flop output at U16J-6, when low, enables one of the four CAS gates, U15H-3, -6, -8, or -11, as selected by the CAS decoding logic.

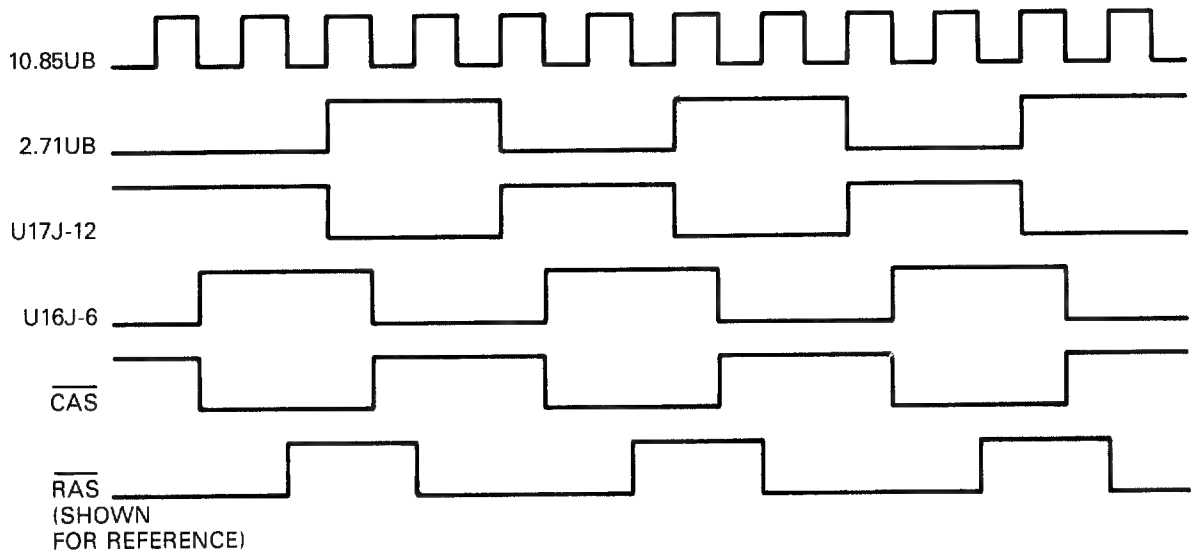


Figure 3-3. CAS Generation Timing Diagram

The CAS decoder output is selected by the Y16 and Y17 bits from the bit slicer logic (U14K-36 and -37, respectively). Flip-flops U16L-9 and U16L-5 are clocked by the U16K-6 signal from the MUX flip-flop. With Y16 and/or Y17 high, the respective flip-flop will be set on the clock pulse. The U16L-9 and U16L-5 outputs are applied to flip-flops U15L-12 and U15L-2, which are clocked by the U15K-5 output from the RAS flip-flop. The U16L-9 and U16L-5 signals are sent to decoder U14J, which decodes the status of the two signals and enables the selected output line. This in turn conditions one of the four CAS output gates for the CAS enabling signal from U16J-6.

INTERFACE SECTION

3.3 CIF/WRITE BOARD (PWB 961346-XXX and 962357-XXX)

The CIF/Write Board performs two independent functions. It contains the circuitry for interfacing the host controller with the Cipher interface, and it provides the write formatting function. The interfacing section is shown on Sheets 1 through 4 of Schematic No. 3; the write formatting logic is shown on Sheets 5 and 6.

Host Controller Interface

Commands, status, and data are exchanged between the host controller and the GCR via the interface section. The interface signals are all active low. The daisy chain is implemented with the pin-to-pin connections of J1 to J1 (Sheet 2). The input signals are received by receivers U4D through U8D. These signals are defined in Table 11. The write data (IW0-IW7, IWP) is latched by write data latch U5E. The write data is clocked into the latch by a Write Strobe (WSTR) from the CIF Write Strobe logic (Sheet 5). The tape drive command lines (IREV, IWRT, IWFM, IEDIT, IERASE, and IHISP) are latched by tape drive command latch U8E, which is clocked by the GO signal when the unit is selected and IGO has been received from the host controller. The command signals are sent to CIO U13F (Sheet 3), and the coding of these commands causes the tape drive to perform specific operations as shown in Table 12.

The unit address is established by the FAD1, FAD2, and FAD3 signals that are latched by U13E (Sheet3) from the CPU bus (AD13, AD14, and AD15). The FAD1, FAD2, and FAD3 signals are applied to XOR gates U5H-1, U5H-9, and U15F-12, respectively (Sheet 2). The status of the interface address signals (IFAD, ITAD0, ITAD1) must enable the three XOR gates to select the unit. (See Table 13 for unit address codes.) When the three XOR gate outputs are high, gate U8K-8 is enabled, conditioning gate U12H-11 for the initiating IGO signal and generating Function Select (FSEL). FSEL enables the output interface drivers (U9D, U9E, U10D, U10E, U11D, and U11E), placing the GCR status signals on the output lines to the host controller.

The IGO signal from the host controller is inverted at U12H-11 and, when active, enables the addressed unit, generating GO. The GO signal latches the command bits into latch U8E and generates an interrupt to the CPU via CIO U13F-15 (Sheet 3) to indicate an interface command. The GO signal also latches the formatter busy state at U6K-5 (Sheet 2). The output signals from the GCR to the host controller are defined in Table 14.

Cache Memory Interface

The CIF/Write Board interfaces with the cache memory via connector J3 (Sheet 4). Write data (MWD0-7) is routed from the host interface to the cache via write data latch U5E (Sheet 2) during a write operation. Read data (MRD0-7, P, Sheet 4) is routed from the cache to the host interface via output drivers U10D, U11D, and U11E (Sheet 2) during a read operation. The transfers are synchronized by using the cache memory clocks. The cache memory is a three-phase read/write memory with automatic address advance. The three phases are Interface, CPU, and Read/Write. The cache memory clocks for these phases are INTERFACE CLK, CPU CLK, and R/W CLK (Sheet 4). The three phases repeat every 1.57 microseconds. The Interface Board accesses the cache during the Interface (ICR) phase, resulting in a 520-nanosecond access every 1.57 microseconds.

The three cache memory clocks are buffered by U1D and are then used by the interface control logic (Sheet 5). The buffered INTERFACE CLK signal also generates the Interface Clock Rate (ICR) signal (Sheet 4), which is used to enable write data buffer U4E for transfer of data to the cache during a write operation. The buffered CPU CLK (CCR) clocks latch U1E to latch the read data after buffering by U2E during a read operation. The CCR clock also clocks the buffered read parity bit (BRDP) into parity check flip-flop U1F.

In the write mode, the cache memory writes whatever data the write data buffer U4E is driving on the lines. If Advance Hold (ADV/H) from the Interface Control logic is high at U7E-2, the cache memory address counter is incremented after the write. If ADV/H is low, continuous writing on each ICR phase occurs to one memory location.

In the read mode, the cache memory transfers whatever data is in the address specified by the address counter to the read buffer (U2E on each ICR phase). If ADV/H is high, the address is incremented; if ADV/H is low, the same address is read during each ICR phase.

CPU Interface

The CPU maintains overall control of the interface logic. Interrupts and interface status information are sent to the CPU via the CIO (U13F, Sheet 3) on the Address/Data lines (AD0-AD7). The CPU sends control signals to the interface via the AD0-AD7 lines to latches U11F, U12F, U13E, and U15E, and decoders U9H and U10H. The CPU bus is interfaced with the CIF/Write Board via octal buffers U14E, U14F, and U15D.

The CIO performs two control functions by means of three internal CIO counters. Two counters are programmed to operate in series, and are initially loaded with the read data word count. Each data transfer is counted via the COUNTER 1 INPUT line at U13F-13, and the counters are decremented. When the counters are decremented to zero, the read data terminal count signal (ITC) is generated at U13F-12, and sent to the CIF control logic. The third internal CIO counter is used by the write formatter to count data groups for the purpose of inserting a resync burst every 158 data groups. The 158 CLK signal from the write formatter is sent to the counter via U13F-20; the terminal count for the 158 data groups (158 TC) is returned to the write formatter from U13-19.

The Test Write Data and Test Read Data latches (U9F and U12E) are used during test operations. The CPU can direct write operations to the CIF/Write Board write data bus or read operations to the read data bus via these latches.

Data Flow

Data flows to and from the host controller on the unidirectional read and write data buses. The interfacing of these buses with the host controller is described in the Cache Memory Interface section. The data flows across the CIF/Write Board unchanged except for the insertion of a parity bit in the write mode. During write operations, the CRC, ACRC, residual, and pad character bytes are inserted by both GCR and PE data. These bytes are inserted by U6F, U7F, U4F, and U3F (Sheet 4) respectively. The data flow and check character insertions are controlled by the state machine (U1J, U1K, U2J, U2K, U3J, and U3K), as described in the Data Flow control discussion.

The ECC byte is accumulated in ECC generator U5F during seven data transfers on the write data bus. The ECC is output to the write data bus during the eighth time period. There is no data transfer during the eighth time period. The ECC generator is reset with a Reset ECC (RECC) pulse from state machine latch U1J on the ECC clock (CECC) for the eighth time period.

The CRC and ACRC characters are generated similarly in generators U6F and U7F respectively. However, these characters are accumulated for a whole block and the generators are output and reset at the end.

The residual character is accumulated in counters U4H and U4J and is gated onto the write data bus by octal buffers U4F at the end of each block. When required, pads are generated and gated onto the write data bus by octal buffers U3F.

Read data operations are also controlled by the state machine (U1J, U1K, U2J, U2K, U3J, and U3K) as described in the Data Flow Control discussion. Read operations for both GCR and PE data are identical. The read data is transferred from cache memory to the interface via the read data bus (RD0-7,P), and to the write formatter via the Buffer Read Lines (RED0-7, P).

Data Flow Control

The CPU initiates read or write operations on the CIF/Write Board by asserting a Start Data Transmission Pulse (SDTP) at output control pulse decoder U9H-9 (Sheet 3). The SDTP pulse sets Data Transmission (DT) at interface data transmission latch U8L-5 in the CIF control logic (Sheet 5). The DT pulse starts the CIF state machine, which consists of three PROMs (U1K, U2K, and U3K, Sheet 4) and three latches (U1J, U2J, and U3J). The state machine controls the data flow and timing for read or write operations. When the Data Transmission is completed, the state machine resets the interface logic. The DT signal is reset by RDT from U1J-16 to interface data transmission latch U8L (Sheet 5). The CPU is notified of the transmission completion by the trailing edge of DT at CIO U13F-32 (Sheet 3).

The state machine also controls the accumulation of check bits, the insertion of the ECC character, and the addition of the CRC and residual data groups. This control is maintained by the three PROMs and the output latches in the form of clock and enabling signals at the latch outputs (U1J, U2J, U3J, Sheet 4).

The interface data transfer rates are controlled by the microprocessor via latch U13E (Sheet 3). The output control codes (CC1 through CC5) are sent to reduced rate counter U13J (Sheet 5). The counter output is gated to produce CNT14, which is routed to the R or W maximum rate gates (U10P) to establish the state Machine Clock (SMCLK). The SMCLK signal clocks the CIF control state machine latches (1J, 2J, 3J, Sheet 4) to control the data transfer rate. The CC1 through CC5 codings and resulting interface data rates are shown in Table 15.

Write Formatter

The Write formatter circuitry (Sheet 6), when initiated by the microprocessor, reads data from the cache memory, performs GCR or PE write data formatting operations, and transmits the data and appended control codes to the head drive circuitry (Sheet 7).

The command synchro circuit, consisting of latches U4M, XOR gate U5H, and associated logic, initiates the operation of the write formatter and synchronizes the

microprocessor output signals to the Cache memory three-phase clock. The write formatter is initiated by the Write Formatter Load Command (WFLC) at U4M-3. WFLC is a negative pulse that clears U4M-9 and then sets U4M-5 on the positive-going trailing edge of the pulse placing a high at U4M-12. The Read Write Clock Rate (RWCR) clock is applied to XOR gate U5H-5 where it is XORed with the inverted Word Formatter Control Bit 3 (WFB3) signal (GCR/PE) from the microprocessor. During a GCR operation (GCR/PE high), the UH5-6 clock pulses occur on the trailing edge of the RWCR clock; during a PE operation (GCR/PE low), the U5H-6 clock pulses occur on the leading edge of the RWCR clock.

The first U5H-6 clock pulse after the WFLC pulse sets latch U4M-9, enabling the Word Formatter Control Bits (WFB0-WFB3) line receivers U2L and clearing latch U4M-5. The second U5H-6 pulse clears latch U4M-9, enabling the latch U1N outputs and initiating the operation of the state controller, consisting of PROMs U1M, U2M, and U3M and latches U1N, U2N, and U3N. The latches are clocked by the U5H-6 clock pulses.

The general operation of the write formatting circuitry is then controlled by the state controller logic. The state controller either PE or GCR write formatting operations, as dictated by the state of Write Formatter Control Bit 3 (WFB3).

For GCR operations, the state controller outputs the 158 CLK signal to the CIO (U13F, Sheet 3) and inserts the 158 resync first when the CIO returns the 158 TC (158 Terminal Count) signal. The state controller produces the timing and control levels for the preamble, postamble, and control codes. The programmable logic arrays (PLA) (U5R through U12R) perform the 4-to-5 conversion, generate codes for the resync burst, the preamble, the postamble, control codes, and modulation for the GCR.

For PE operations, the state controller performs general control for the overall operation, and provides timing and control levels for the preamble, postamble, and control codes. The PLAs generate the codes for the preamble, the postamble, and control codes and performs part of the PE modulation. The balance of the PE modulation is done with flip-flops (two per channel) in the write drive circuitry (Sheet 7).

3.4 DATA BOARD (PWB 961420-XXX)

The Data Board contains PE and GCR read amplifiers and read formatting logic. The read heads interface directly with the Data Board. The board provides the following functions:

- Read Data Detection and Amplification
- Read Data and Read Clock Recovery
- Read State Machine Control
- Read Data Deskew Buffering
- GCR Read Data Five-Bit to Four-Bit Conversion
- Read Channel Error Logging

The Data Board contains the following logic circuits to perform these functions:

- Read Amplifier
- Phase Lock Loop
- Deskew Buffer Logic
- Channel State Machine
- Master State Machine

- o Clock Generation Logic
- o Block Detection Logic
- o Cache Bus Interface

The handling of both PE and GCR density read data is common for the Read Amplifier, Phase Lock Loop, and Deskew Logic. Data from each of the nine channels is handled independently through the Deskew Logic, and is then aligned into 9-bit characters and synchronously clocked into the cache memory. The Channel State Machine is each channel controls the read format functions, and the Master State Machine directly controls the Channel State Machines. The Master State Machine is, in turn, controlled by the microprocessor located on the CPU/MMU Board.

A detailed description of each of the Data Board logic circuits follows. Refer to Schematic No. 4.

Read Amplifier

The Read Amplifier (Sheets 2, 3, 4) is a semi-custom device that integrates all read data amplification functions for one complete channel. A separate Read Amplifier is used for each of the nine read data channels. The following discussion covers the Read Amplifier (U15K) data channel 2 (Sheet 2). The Read Amplifiers for the remaining channels function identically.

Inputs from the read head (RPHD and RMHD) are received at pins 21 and 22 respectively. The Voltage Comparator (VCOM) signal at pin 7, from the Digital-to-Analog Converter (DAC) on the Sense/Servo Board, sets the threshold level for the detection of flux transitions. The RDROP2 signal indicates that a flux tansition has not been detected for four consecutive read times, and is sent to the Voltage-Controlled Oscillator (VCO) in the Phase Lock Loop to halt the read operation and generate a channel error signal. The RDPLS2 signal occurs on each detected transition, and is sent to the VCO to indicate that a transition has occurred. The RDATA2 signal is sent to the skew test point logic (Sheet 2) for skew summing.

Phase Lock Loop

The Phase Lock Loop (Sheets 5 through 13) receives the detected flux transition signal from the Read Amplifier and, through a group of one-shot multivibrators and associated logic devices, conditions the signal for the deskew logic. As in the case of the Read Amplifiers, a separate Phase Lock Loop is used for each of the nine channels. The following discussion covers the Phase Lock Loop for the channel 2 (Sheet 8). The Phase Lock Loops for the remaining channels function identically.

A VCO, together with associated components, continually cycles to provide a phase reference for the read signal. The frequency of the VCO is initially set by potentiometer R519. When in the GCR mode, the low P/G signal enables FETs U14J, which change the charge on capacitors C508, C509, C503,and C504 to speed up the frequency of the VCO.

A flux transition is indicated by a low RDPLS2 signal from the read amplifier. This signal turns on multivibrator U14K-13, which sends a high to the CLR input of latch U12K-13, enabling the latch. If the flux transition has occurred before U14K-5 in the VCO has been turned on, U12K is clocked by the U14K-12 signal, sending a low from U12K-8 to the pump down (PD) input of U12J. This indicates a data early condition. If U14K-5 in the VCO is turned on before the RDPLS2 signal is received, U12K is clocked

by U14K-4 signal when RDPLS2 is received, sending U12K-6 low. The U12K-6 signal is applied to the pump up (PU) input of U12J to indicate a data late condition.

The PU or PD input to U12J causes the output at U12J-8 to increase or decrease, respectively. This changes the voltage levels to the VCO components, increasing or decreasing the frequency of the VCO in accordance with the data early or data late condition.

When U14K-13 is turned on by the RDPLS2 signal, the low at U14K-4, indicating a flux transition, clocks latch U11K-5, setting the latch. Multivibrator U13K-5, when turned on by the VCO, clocks the data bit into latch U11K-12 synchronizing the read pulse with the VCO and producing Synchronized Data (SD) at U11K-9.

When the RDROP2 signal is active (low), indicating that a flux transition has not been detected for four character read times, an error condition is signalled. This error condition is common to both PE and GCR recording techniques, since in PE a flux transition occurs at each read time, and in GCR, no more than two consecutive zeros can occur. The RDROP2 signal holds U14K-13 clear, and signals a channel error to the channel state machine via gate U9K-6 and latch U10D-7.

Deskew Buffer Logic

The SD bits are sent to FIFO buffers U10J and U9J. Each FIFO is 16 bits deep. When FIFO U9J is full, it sends a low Channel Read (CHRDY2) signal to the master state logic to indicate that data is ready for transfer. The FIFO is clocked by the FIFOCLK from the clock generation logic, which is common to all channels, when gate U9K-11 is enabled by ENAFIFO from the channel state logic. The data is transferred serially to latches U8J in the channel state machine.

When FIFO U9J is full, the SD bits are accumulated in FIFO U10J. If the data is not transferred from U9J, and U10J becomes full, the signal from U10J-2 (IR) becomes active (low), signalling an error condition. Latch U10K-5 is reset on the next RDC clock pulse from the phase lock loop, generating an OVERFLOW signal. The OVERFLOW signal initiates a channel error signal in the channel state logic via gate U9K-6 and latch U10D-7.

Channel State Machine

The channel state machine consists of latches U8J, PROM U7J, and associated logic. The channel state machine is controlled by A, B, and C signals from the master state machine to PROM U7J, which dictate the method by which the data is processed and output. The channel state machine can detect an end mark (ENDMK), which would not be output on the cache bus, a MK2, a PE postamble (PEP2), or data. When data is specified, it is processed by the channel state machine and output to the master state machine for transfer on the cache bus. The channel state machine also performs the 5-to-4-bit conversion function for GCR data.

The U8J latches are clocked by State Clock A (STCLKA) from the clock generation logic, and receive the data serially from the deskew buffer logic at U8J-17. When PROM U7J is instructed by signals, A, B, and C from the master state machine that a GCR data transfer is occurring, the first data bit received by U7J and U8J is shifted upward and returned to U8J-3 on the next clock pulse. Each data bit is similarly shifted upward until the fifth data bit is received. PROM U7J then shifts four data bits out serially to gate U18K-1, to generate SRDATA2 at U8K-3. The decoded data is sent to the cache bus interface logic for transfer to the cache.

When a channel error is detected, PROM U7J receives the error indication signal at U7J-1, and generates the CHERR2 signal at U8M-11. When the data pattern received by PROM U7J indicates an end mark or a MK2/PEP2, the resulting signals are generated at U8M-10 and -9 respectively. The CHERR2, EMK2, and MK2/PEP2 signals are sent to the master state machine logic.

Master State Machine

The master state machine (Sheet 14) controls the processing of the individual channels via the A, B, and C signals, and generates flags to the CPU to indicate format and status. The master state machine consists primarily of voting PROMs U5J, U6H, and U6G; EPROMs U3G and U4G; CIO U5B; and related gates, latches, and processing logic.

The channel ready (CHRDY0 - CHARDY7, CHRDYP) signals are latched at U6J and U5H, and sent to voting PROM U5J. When a minimum of seven channels indicate a ready condition via the respective channel ready signals, voting PROM U5J generates Data Ready (DRDY). DRDY is sent to EPROMs U3G and U4G via latch U4H-12 to indicate that data is ready to be transferred in all deskew buffer logic FIFOs.

Similarly, End Marks (EMK0 - EMK7, EMKP) and Mark 2/PE postamble detected (MK2/PE0 - MK2/PEP7, MK2/PEPP) inputs from the individual channels are received by voting PROMs U6H and U6G, respectively. When PROM U6H detects a minimum of seven channels specifying an End Mark, or PROM U6G detects a minimum of seven channels specifying a MK2 or PE postamble detected, the respective PROM generates an EMK/PE0 or MK2/PE1 signal.

A priority encoder (U5G) receives EMK/PE0 and MK2/PE1 Block Detect Delay (BLKDY), as well as, Block Detect (BLOCK DET), and Pad Count (PADCNT). The ENMASTER signal is generated by the CPU and routed to latch U4H via CIO U5B. This signal is used to enable the master state machine during a read operation. The BLOCK DET signal is sent from the block detect logic to indicate that data has been detected and that read operations should be initiated by the master state machine. BLOCK DET enables the operation of the priority encoder. The PADCNT signal is generated during PE operations and is used to pad the eighth character during a PE read function.

Priority encoder U5G encodes the five input signals to enable output line A0 or A1. These lines, via XOR gates U1G-3 and -6, are latched by U4H, which also latches status signals Data Ready (DRDY) from voting PROM U5J, FWD/REV from the CPU via CIO U5B, and PE/GCR, also from the CPU via the CIO.

These signals are sent to master state machine EPROMs U3G and U4G. The EPROMs generate control signals A, B, and C to the channel state machines via latches U1H, and format/status signals to the CPU via latch U2H and the CIO.

The CIO communicates with the CPU via the bi-directional CPU bus consisting of lines AD0-AD7. These lines are buffered by buffers U6A and are routed to and from the CPU/MMU Board via connector J5. Control signals for the CIO are received via connector J5 and buffers U5A. The status and control signals sent between the CPU and the Data Board via the CIO are listed and described in Table 16.

The synchronized read data (SRDATA0-SRDATA7) from the individual channels is latched at U4C and routed to the cache bus interface logic via buffered read data lines BRDATA0-BRDATA7. The parity bit (SRDATAP) is latched at U4E-9 and routed to the cache bus interface via the BRDATAP line.

Clock Generation Logic

The clock generation logic (Sheet 15) receives four clock signals from the MMU portion of the CPU/MMU Board via connector J3 (Sheet 14), as follows:

- CLD542 - The 5.42-MHz clock
- CLK271 - The 2.71-MHz clock
- R/WCKL - The read/write clock
- CPUCLK - The basic CPU clock signal

The clock generation logic (Sheet 15) synchronizes these four clocks to produce five basic clock signals that are used to control the operations of the data board. These five clocks are the FIFOCLK, CLK542, and master state machine clocks A, B, and C (STCLKA, STCLKB, and STCLKC).

Block Detection Logic

The block detection logic detects recorded tape and signals the master state machine and the CPU via the BLOCK DET line. The RDROP0 - REDOP7 and RDROPP signals from the read amplifier are received by PROM U6F-1. When data is detected on one or more of the channels, the respective RDROP signal is high. When no data is detected, all RDROP signals are low, and the U6F-1 PROM output holds flip-flop U4F reset via amplifier network U5F-13. This holds the BLOCK DET signal low, indicating that no data is recorded on the tape. When one or more of the RDROP signals is high, flip-flop U4F-10 is set, sending BLOCK DET high to indicate that recorded data is present on the tape.

Cache Bus Interface

The cache bus interface logic consists of nine gates (U3C, U4B, and U3B), line drivers U4A, and parity checker U3A. The gates are enabled by the high PEPAD signal from the master state machine. The gates receive the Buffered Read Data (BRDATA0 - BRDATA7, and BRDATAP) from the master state machine logic. When the gates are enabled by PEPAD, the data is routed via the line drivers and connector J3 to the cache on the MWD0 - MWD7, MWDP lines. During PE operation the PEPAD signal goes low every eight character count, inhibiting the gates and placing all zeroes on the output lines.

Parity checker U3A receives the BRDATA0 - BRDATA7, BRDATATAP signals and checks for a parity error. If an error is detected, Vertical Redundancy Check Error (VRCERR) is generated and sent to the CPU via CIO U5B (Sheet 14) to flag the error.

3.5 SENSE/SERVO BOARD (PWB 962832-XXX and 962810-XXX)

The Sense/Servo Board is a multiple-function PWB that contains the following circuits:

- Voltage sourcing and regulation
- Sensor signal processing
- Mechanical actuations/drivers
- Erase/Write Head drive
- Compliance arm position sensing
- Analog-to-Digital Converter
- Supply reel servo driver
- Take-up reel servo driver

- o Operator Panel interface
- o Alphanumeric Display Panel interface
- o Communication control

All top plate connections, except for data to and from the head, are made through the Sense Servo Board. The board provides voltage for all other system boards, and all direct external communications are made through the board via the Operator Control Panel, Alphanumeric Display Panel, or Serial Interface.

The following detailed descriptions of the Sense/Servo Board functions are based on Schematic No. 5. All sheet number references in the description refer to sheet numbers of that figure.

Voltage Sourcing and Regulation (See Sheet 2)

Voltage sourcing and regulation is performed on the Sense/Servo Board. Unregulated input voltages are received from Power Supply Module PS1 via connector J1. A 3525A integrated circuit (U5G) is used to achieve switching regulation. The switching frequency of 25 kHz is determined by resistor R59 and capacitor C54. The 3525A drives a push-pull power stage consisting of transistors Q1, and Q2, which actuate current boost transformer T1.

Voltage regulation is taken from the secondary of the transformer T1 5-volt tap after frequency filtering through inductor L4 and capacitor C6. The +5-volt transformer output is rectified and sent to all system logic via connector P4.

Monitoring of the unregulated 57V dc input is done through comparator U3E. If the input drops below 38V dc, U3E will shut down the switching regulator U5G. In addition, one-shot U5E will send a power-on reset signal (PWR RES) to the microprocessor when power is applied.

Sensor Signal Processing (See Sheet 3)

The sensor input signals are received at J7 and J8, and consist of the following:

- o Take-up reel tachometer
- o Door sensor
- o File protect sensor
- o Beginning-of-tape (BOT) sensor
- o End-of-tape (EOT) sensor
- o Tape-in-path sensor

The sensor input signals are detected, shaped, and processed through comparators U2K and U16H. The resulting TTL-compatible signals, with the exception of the tachometer outputs, are fed directly to CIO U6A (Sheet 7) for processing by the microprocessor. The tachometer outputs (TP0 and TP1) are pulse-shaped and conditioned by U11E and U12H (Sheet 7) before being routed to the CIO.

Mechanical Actuators/Drivers (See Sheet 3)

The following functions are controlled by the Sense/Servo Board:

- o Blower motor
- o Door lock solenoid
- o Hub lock solenoid

The Blower (BLWR), Door Lock (DRLK), and Hub Lock (HBLK) signals are sent from the microprocessor via CIO U14A (Sheet 7). The BLWR signal controls the blower motor through transistor Q8; the DRLK signal controls the door lock solenoid through driver U9H-4 and transistor Q14; and the HBLK signal controls the hub lock solenoid through driver U9E-8 and transistor Q10.

Erase/Write Head Drive Circuits (See Sheet 3)

The system uses three separate magnetic head assemblies; the erase head, the early erase head, and the write head. The drive circuits for these heads are located on the Sense/Servo Board. The drive circuits are controlled by signals from the microprocessor sent via CIO U14A (Sheet 7). The Erase Head 1 Enable (EH1EN) signal controls the operation of the erase head drive circuitry, which consists of driver U7C-12, transistor Q7, and related discrete components. The Write Enable (WEN) and 6250 signal control the operation of the write center tape head drive circuitry, which consists of transistors Q9, Q10, Q50, and Q51; and related discrete components.

Compliance Arm Position Sensing (See Sheet 3)

Signals indicating the position and rate of change of position of the compliance arm are generated by the compliance arm sensing logic. The compliance arm drive signal is derived from the 40 kHz SERVCLK output of CIO U14A-19 (Sheet 7) by drivers U16N-4 and -6; operational amplifiers U16K-12 and -6; and related discrete components. A variable capacitor couples the compliance arm sense signal (ARMSNS) to U16K-6, where the arm position (ARMPOS) signal is generated. The ARMPOS signal is routed to the Analog-to-Digital Converter (Sheet 4) via multiplexer U10E. The ARMPOS signal is also applied to differentiation circuit at U16K-8, consisting of U16K-10, U16L-4 and related discrete components. The output at U16K-3, Arm Division (ARMDIV), is also sent to the Analog-to-Digital Converter (Sheet 4) via multiplexer U10E to indicate the rate of change of the position of the compliance arm.

Analog-to-Digital Converter (See Sheet 4)

The Analog-to-Digital Converter (ADC) provides communications between various analog signals and the microprocessor. The ADC consists of ADC1001 (U13E) and two 4051 multiplexer (U10E). The following analog lines are multiplexed and digitized for transmission to the microprocessor:

- +12V
- -12V
- +5V
- +57V
- Write Center Tap Voltage (WCTV)
- Take-up Motor Voltage/Current (TMV/TMI)
- Supply Motor Voltage/Current (SMV/SMI)
- Arm Division (ARMDIV)
- Arm Position (ARMPOS)

The signal to be sampled is selected by the A, B, C address signals from CIO U14A. The selected signal, after digitizing by U13E is routed to the microprocessor on the higher order byte of the processor address/data bus (AD8-AD15).

Digital-to-Analog Converter (See Sheet 4)

The Digital-to-Analog Converter (DAC) provides communication between the microprocessor bus and various analog signals. The DAC consists U12A, a 4051 demultiplexer (U10A), differential amplifiers (U11A-1 and U11A-7), voltage followers (U8A and U8B), and related discrete components. The following analog functions are generated by the DAC:

- o Supply Motor Current (ISU)
- o Take-up Motor Current (ITU)
- o Read Amplifier Voltage Threshold (ITHR)

The DAC receives bits AD6 and AD7 and the high order byte (AD8-AD15) of the processor address/data bus. The analog output is available at U11A-7, and is sent to demultiplexer U10A for selection. The demultiplexer is enabled by the MDAC signal from CIO U14A-33 (Sheet 7), and the output signal of the demultiplexer is selected by the A, B, C address signals from U14A-32, -31, and -30. The selected demultiplexer output signal is clamped by one of the high impedance voltage followers (U8A or U8B). The selected output charges the associated capacitor (C71 through C73 and C266) to the desired value, and since the demultiplexer output returns to a very high impedance state, the capacitor retains that value until the next refresh time.

Supply Reel Servo Driver (See Sheet 5)

The ISU signal from the DAC (Sheet 4) is the drive signal (supply current) for the supply reel servo driver. The ISU signal is applied to U15S where it is filtered. The signal is then modulated by a 20 kHz sawtooth (f+ and f-) at comparators U15T. The sawtooth is generated by U15R and U15S from a 40 kHz Servo Clock (SERVCLK) signal initiated by CIO U14A-19 (Sheet 7). The pulse-width-modulated signals from U15T-1 and U15T-2 are applied to the gating network of U7T. If the ISU signal was negative, specifying forward reel movement, the signals from U17T-6 and U17T-8 are sent to driver transistors Q44 and Q45. The ISU was low, specifying reverse reel movement, the phase difference will result in reverse motion. The driver transistors feed an H-bridge power driver comprised of transistors Q35, Q36, Q37, Q38, and their related components, which drive the supply motor through inductors L8 and L9 and motor breaking relay K1. Voltage feedback is provided by comparator U6W-3, which generates the Servo Motor Voltage (SMV) signal that is sent to the Analog-to-Digital Converter (Sheet 4) for digitizing and routing to the microprocessor. Current feedback is provided by U6W-10, which generates Servo Motor Current (SMI) for routing to the microprocessor via the Analog-to-Digital Converter.

Current limit protection is provided by comparator network U8W. When the servo motor current exceeds its maximum limit, the High Current (HII) signal at U17R-4 (Sheet 6) goes low. This inhibits the U17T gating network, causing the servo drive to shut down.

Further shutdown protection is provided by the Watchdog Timer logic (Sheet 6). If the +5V drops too low, the Servo Enable 2 (SERV EN 2) signal at U17S-8 goes low. This shuts off transistor Q11, deenergizing relay K1 and shutting down the servo drive.

Take-up Reel Servo Driver (See Sheet 6)

The operation of the take-up reel servo driver is similar to that of the supply reel servo driver. The ITU signal from the DAC (Sheet 4) is the drive signal (supply current) for

the take-up reel servo driver. The ITU signal is applied to U15V-6 where it is filtered. The signal is then modulated by the 20 kHz sawtooth (f+ and f-) from the supply reel servo driver logic at comparators U15P. The pulse-modulated signals from U15P-13 and U15P-14 are applied to the gating network of U17P-9 and U17P-3. If the ITU signal was negative, specifying forward reel movement, the signals from U17T-6 and U17T-8 are sent to driver transistors Q40 and Q41; the phase difference will result in forward motion. The driver transistors feed an H-bridge power driver comprised of transistors Q31, Q32, Q33, Q34, and their related components, which drive the take-up motor through inductors L7 and L6 and motor breaking relay K1. Voltage feedback is provided by comparator U6W-4, which generates the Take-up Motor Voltage (TMV) signal that is sent to the Analog-to-Digital Converter (Sheet 4) for digitizing and routing to the microprocessor. Current feedback is provided by comparator U6W-12, which generates Take-up Motor Current (TMI) for routing to the microprocessor via the Analog-to-Digital Converter.

Current limit protection is provided by comparator network U8W. When the Take-up Motor Current exceeds its maximum limit, the High Current (HII) signal at U17R-4 goes low. This inhibits the U17P gating network, causing the take-up servo drive to shut down.

The take-up motor drive also has the further shutdown protection of the Watchdog Timer logic detailed in the description of the Supply Reel Servo Driver.

Operator Panel Interface (See Sheet 4)

The Sense/Servo Board processes control signals that operate a power switch, a power on indicator, and six tactile membrane switches with five associated light emitting diodes (LEDs) on the Operator Control Panel. The LEDs are controlled by the LOAD, UNLOAD, ON-LINE, WRT EN, and HI DEN signals from CIO U16A (Sheet 7) through drivers U15E. The switches are sensed by a resistor divider circuit and the same CIO lines that drive the LEDs.

Alphanumeric Display Panel Interface (See Sheet 7)

The Alphanumeric Display Panel contains an eight-character (ASCII) fourteen-segment display and three density display LED bars. When the alphanumeric display or LED display address is decoded by U12E (DSPSL or LEDSL, respectively), data is sent to the selected display via drivers U14E and U14F on the BAD0-BAD5 lines.

Communication Control (See Sheet 7)

Communications between the Sense/Servo Board and the microprocessor is accomplished by reading and writing to memory locations corresponding to six memory-mapped input/output devices. These devices are the two CIOs (U14A and U16A), the Analog-to-Digital Converter (U13E), the Digital-to-Analog Converter (U12A), and the density and alphanumeric displays located on the Alphanumeric Display Panel. Addresses within the Sense/Servo Board memory space are latched by latch U12C and decoder by U12E. After decoding, the active output of U12E enables the selected I/O device.

3.6 DATA BOARD (PWB 962789-XXX)

The Data Board contains PE and GCR read amplifiers and read formatting logic. The read heads interface directly with the Data Board. The board provides the following functions:

- o Read Data Detection and Amplification
- o Read Data and Read Clock Recovery
- o Read State Machine Control
- o Read Data Deskew Buffering
- o GCR Read Data Five-Bit to Four-Bit Conversion
- o Read Channel Error Logging

The Data Board contains the following logic circuits to perform these functions:

- o Read Amplifier
- o Phase Lock Loop
- o Deskew Buffer Logic
- o Channel State Machine
- o Master State Machine
- o Clock Generation Logic
- o Block Detection Logic
- o Cache Bus Interface

The handling of both PE and GCR density read data is common for the Read Amplifier, Phase Lock Loop, and Deskew Logic. Data from each of the nine channels is handled independently through the Deskew Logic, and is then aligned into 9-bit characters and synchronously clocked into the cache memory. The Channel State Machine in each channel controls the read format functions, and the Master State Machine directly controls the Channel State Machines. The Master State Machine is, in turn, controlled by the microprocessor located on the CPU/MMU Board.

A detailed description of each of the Data Board logic circuits follows. Refer to Schematic No. 6.

Read Amplifier

The Read Amplifier (Sheets 2, 3, 4) is a semi-custom device that integrates all read data amplification functions for one complete channel. A separate Read Amplifier is used for each of the nine read data channels. The following discussion covers the Read Amplifier (U26K) data channel 2 (Sheet 2). The Read Amplifiers for the remaining channels function identically.

Inputs from the read head (RPHD and RMHD) are received at pins 21 and 22 respectively. The Voltage Comparator (VCOM) signal at pin 7, from the Digital-to-Analog Converter (DAC) on the Sense/Servo Board, sets the threshold level for the detection of flux transitions. The RDROP2 signal indicates that a flux tansition has not been detected for four consecutive read times, and is sent to the Voltage-Controlled Oscillator (VCO) in the Phase Lock Loop to halt the read operation and generate a channel error signal. The RDPLS2 signal occurs on each detected transition, and is sent to the VCO to indicate that a transition has occurred. The RDATA2 signal is sent to the skew test point logic (Sheet 2) for skew summing.

Phase Lock Loop

The Phase Lock Loop (Sheets 5 through 13) receives the detected flux transition signal from the Read Amplifier and, through a group of one-shot multivibrators and associated logic devices, conditions the signal for the deskew logic. As in the case of the Read Amplifiers, a separate Phase Lock Loop is used for each of the nine channels. The following discussion covers the Phase Lock Loop for the channel 2 (Sheet 8). The Phase Lock Loops for the remaining channels function identically.

A VCO, together with associated components, continually cycles to provide a phase reference for the read signal. The frequency of the VCO is initially set by potentiometer R519. When in the GCR mode, the low P/G signal enables FETs U25J, which change the charge on capacitors C508, C509, C503,and C504 to speed up the frequency of the VCO.

A flux transition is indicated by a low RDPLS2 signal from the read amplifier. This signal turns on multivibrator U25K-13, which sends a high to the CLR input of latch U23K-13, enabling the latch. If the flux transition has occurred before U25K-5 in the VCO has been turned on, U23K is clocked by the U25K-12 signal, sending a low from U23K-8 to the pump down (PD) input of U23J. This indicates a data early condition. If U25K-5 in the VCO is turned on before the RDPLS2 signal is received, U23K is clocked by U25K-4 signal when RDPLS2 is received, setting U23K-5 and sending U23K-6 low. The U23K-6 signal is applied to the pump up (PU) input of U23J to indicate a data late condition.

The PU or PD input to U23J causes the output at U23J-8 to increase or decrease, respectively. This changes the voltage levels to the VCO components, increasing or decreasing the frequency of the VCO in accordance with the data early or data late condition.

When U25K-13 is turned on by the RDPLS2 signal, the low at U25K-4, indicating a flux transition, clocks latch U22K-5, setting the latch. Multivibrator U24K-5, when turned on by the VCO, clocks the data bit into latch U22K-12, synchronizing the read pulse with the VCO and producing Synchronized Data (SD) at U22K-9.

When the RDROP2 signal is active (low), indicating that a flux transition has not been detected for four character read times, an error condition is signalled. This error condition is common to both PE and GCR recording techniques, since in PE a flux transition occurs at each read time, and in GCR, no more than two consecutive zeros can occur. The RDROP2 signal holds U25K-13 clear, and signals a channel error to the channel state machine via gate U9K-6 and latch U10D-7.

Deskew Buffer Logic

The SD bits are sent to FIFO buffers U21H and U20H. Each FIFO is 16 bits deep. When FIFO U20H is full, it sends a low Channel Read (CHRDY2) signal to the master state logic to indicate that data is ready for transfer. The FIFO is clocked by the FIFOCLK from the clock generation logic, which is common to all channels, when gate U9K-11 is enabled by ENAFIFO from the channel state logic. The data is transferred serially to latches U8J in the channel state machine.

When FIFO U20H is full, the SD bits are accumulated in FIFO U21H. If the data is not transferred from U20H and U10J becomes full, the signal from U21H-2 (IR) becomes active (low), signalling an error condition. Latch U21J-5 is reset on the next RDC clock pulse from the phase lock loop, generating an OVERFLOW signal. The OVERFLOW signal initiates a channel error signal in the channel state logic via gate U20J-6 and latch U21D-7.

Channel State Machine

The channel state machine consists of latches U19H PROM U18J and associated logic. The channel state machine is controlled by A, B, and C signals from the master state machine to PROM U18J which dictate the method by which the data is processed and

output. The channel state machine can detect an end mark (ENDMK), which would not be output on the cache bus, a MK2, a PE postamble (PEP2), or data. When data is specified, it is processed by the channel state machine and output to the master state machine for transfer on the cache bus. The channel state machine also performs the 5-to-4-bit conversion function for GCR data.

The U19H latches are clocked by State Clock A (STCLKA) from the clock generation logic, and receive the data serially from the deskew buffer logic at U19H-7. When PROM U18J is instructed by signals, A, B, and C from the master state machine that a GCR data transfer is occurring, the first data bit received by U18J and U19H is shifted upward and returned to U19H-3 on the next clock pulse. Each data bit is similarly shifted upward until the fifth data bit is received. PROM U18J then shifts four data bits out serially to gate U18K-1, to generate SRDATA2 at U8K-3. The decoded data is sent to the cache bus interface logic for transfer to the cache.

When a channel error is detected, PROM U18J receives the error indication signal at U18J-1, and generates the CHERR2 signal at U19M-11. When the data pattern received by PROM U18J indicates an end mark or a MK2/PEP2, the resulting signals are generated at U19M-10 and -9 respectively. The CHERR2, EMK2, and MK2/PEP2 signals are sent to the master state machine logic.

Master State Machine

The master state machine (Sheet 14) controls the processing of the individual channels via the A, B, and C signals, and generates flags to the CPU to indicate format and status. The master state machine consists primarily of voting PROMs U12J, U15H, and U15G; EPROMs U5G and U10G; CIO U12B; and related gates, latches and processing logic.

The channel ready (CHRDY0 - CHARDY7, CHRDYP) signals are latched at U15J and U12H, and sent to voting PROM U12J. When a minimum of seven channels indicate a ready condition via the respective channel ready signals, voting PROM U12J generates Data Ready (DRDY). DRDY is sent to EPROMs U5G and U10G via latch U10H-12 to indicate that data is ready to be transferred in all deskew buffer logic FIFOs.

Similarly, End Marks (EMK0 - EMK7, EMKP) and Mark 2/PE postamble detected (MK2/PE0 - MK2/PEP7, MK2/PEPP) inputs from the individual channels are received by voting PROMs U15H and U15G, respectively. When PROM U15H detects a minimum of seven channels specifying an End Mark, or PROM U15G detects a minimum of seven channels specifying a MK2 or PE postamble detected, the respective PROM generates an EMK/PE0 or MK2/PE1 signal.

A priority encoder (U12G) receives EMK/PE0 and MK2/PE1 Block Detect Delay (BLKDY), as well as, Block Detect (BLOCK DET), and Pad Count (PADCNT). The ENMASTER signal is generated by the CPU and routed to latch U12G via CIO U12B. This signal is used to enable the master state machine during a read operation. The BLOCK DET signal is sent from the block detect logic to indicate that data has been detected and that read operations should be initiated by the master state machine. BLOCK DET enables the operation of the priority encoder. The PADCNT signal is generated during PE operations and is used to pad the eighth character during a PE read function.

Priority encoder U12G encode the five input signals to enable output line A0 or A1. These lines, via XOR gates U1G-3 and -6, are latched by U10H, which also latches status signals Data Ready (DRDY) from voting PROM U12J, FWD/REV from the CPU via CIO U12B, and PE/GCR, also from the CPU via the CIO.

These signals are sent to master state machine EPROMs U5G and U10G. The EPROMs generate control signals A, B, and C to the channel state machines via latches U1H, and format/status signals to the CPU via latch U3H and the CIO.

The CIO communicates with the CPU via the bi-directional CPU bus consisting of lines AD0-AD7. These lines are buffered by buffers U15A and are routed to and from the CPU/MMU Board via connector J5. Control signals for the CIO are received via connector J5 and buffers U12A. The status and control signals sent between the CPU and the Data Board via the CIO are listed and described in Table 16.

The synchronized read data (SRDATA0-SRDATA7) from the individual channels is latched at U10C and routed to the cache bus interface logic via buffered read data lines BRDATA0-BRDATA7. The parity bit (SRDATAP) is latched at U10E-9 and routed to the cache bus interface via the BRDATAP line.

Clock Generation Logic

The clock generation logic (Sheet 15) receives four clock signals from the MMU portion of the CPU/MMU Board via connector J3 (Sheet 14), as follows:

- CLD542 - The 5.42-MHz clock
- CLK271 - The 2.71-MHz clock
- R/WCKL - The read/write clock
- CPUCLK - The basic CPU clock signal

The clock generation logic (Sheet 15) synchronizes these four clocks to produce five basic clock signals that are used to control the operations of the data board. These five clocks are the FIFOCLK, CLK542, and master state machine clocks A, B, and C (STCLKA, STCLKB, and STCLKC).

Block Detection Logic

The block detection logic detects recorded tape and signals the master state machine and the CPU via the BLOCK DET line. The RDROP0 - REDOP7 and RDROPP signals from the read amplifier are received by PROM U15F. When data is detected on one or more of the channels, the respective RDROP signal is high. When no data is detected, all RDROP signals are low, and the U15F PROM output holds flip-flop U10F reset via amplifier network U12F-13. This holds the BLOCK DET signal low, indicating that no data is recorded on the tape. When one or more of the RDROP signals is high, flip-flop U10F-10 is set, sending BLOCK DET high to indicate that recorded data is present on the tape.

Cache Bus Interface

The cache bus interface logic consists of nine gates (U6C, U10B, and U6B), line drivers U10A, and parity checker U6A. The gates are enabled by the high PEPAD signal from the master state machine. The gates receive the Buffered Read Data (BRDATA0 - BRDATA7, and BRDATAP) from the master state machine logic. When the gates are enabled by PEPAD, the data is routed via the line drivers and connector J3 to the cache on the MWD0 - MWD7, MWDP lines. During PE operation the PEPAD signal goes low every eight character count, inhibiting the gates and placing all zeroes on the output lines.

Parity checker U6A receives the BRDATA0 - BRDATA7, BRDATATAP signals and checks for a parity error. If an error is detected, Vertical Redundancy Check Error (VRCERR) is generated and sent to the CPU via CIO U12B (Sheet 14) to flag the error.

TABLES

CHAPTER 4.

Data values 1234/5678	Record values 12345/678910
0000	11001
0001	11011
0010	10010
0011	10011
0100	11101
0101	10101
0110	10110
0111	10111
1000	11010
1001	01001
1010	01010
1011	01011
1100	11110
1101	01101
1110	01110
1111	01111

Table 1. GCR Four-To-Five Bit Translation Codes

ANSI Channel	Data A	Subgroups B	Storage A	Subgroups B
1	DDDD	DDDE	XXXXX	XXXXX
2	DDDD	DDDE	XXXXX	XXXXX
3	DDDD	DDDE	XXXXX	XXXXX
4	PPPP	PPPP	XXXXX	XXXXX
5	DDDD	DDDE	XXXXX	XXXXX
6	DDDD	DDDE	XXXXX	XXXXX
7	DDDD	DDDE	XXXXX	XXXXX
8	DDDD	DDDE	XXXXX	XXXXX
9	DDDD	DDDE	XXXXX	XXXXX
Group Position	1234	5678	12345	678910

LEGEND: D: Data Bit
P: Vertical Parity Bit
E: Error Correction Code
X: 4 To 5 Conversion Code

Table 2. Data Group To Storage Group Format

HIGH BYTE (Sheet 4)	LOW BYTE (Sheet 5)
U23M, U26M, U26P, U26N, U24M, U24N, U23P, U23N, U24P	U19M, U19N, U19P, U21M, U21N, U21P, U22M, U22N, U22P

Table 3. DRAM Locations

ST3	ST2	ST1	ST0	Operation	U23C Active Line
0	0	0	1	Memory refresh	REFRESH
0	0	1	0	I/O reference	IO
0	0	1	1	Special I/O reference	SPECIAL IO
0	1	1	1	Interrupt acknowledge	INTA
1	0	0	0	Data memory request	DATA
1	0	0	1	Stack memory request	STACK

Table 4. Microprocessor Status Line Codes

SIGNAL	FUNCTION
$\overline{\text{SCIO}}$ (Select CIO)	Sent to CPU (Sheet 2); used to select Xmit mode for U23F and U25F (BAD0-15). Selects CIO U20D (Sheet 7).
$\overline{\text{SNRM}}$ (Select NOVRAM)	Sent to NOVRAM U25J (Sheet 6) to select the NOVRAM.
$\overline{\text{STORE NR}}$ (Store NOVRAM)	Initiates a store operation in the NOVRAM (25J, Sheet 6).
$\overline{\text{RECALL NR}}$ (Recall NOVRAM)	Initiates an array recall operations in the NOVRAM.
($\overline{\text{R BOOT}}$ (Reset Boot)	Used by boot control logic (Sheet 3) to generate $\overline{\text{BOOT}}$ after power test.
$\overline{\text{CDATA}}$ (Cache Data)	Indicates that an operation involving cache data is occuring.
$\overline{\text{CADD}}$ (Cache Address)	Sent to U22H to start cache address transmission to the DMA.

Table 5. DMA Control Address Decoder Signal Functions

PIN NO. (U20D-)	SIGNAL NAME	SOURCE/DESTINATION	FUNCTION
6	R/W	$\overline{ZR/W}$ From CPU (Sheet 2)	High: Read to CPU Low: Write to CIO
36	$\overline{CS0}$	$\overline{SCIO}$ From Address Decoder U27J (Sheet 7)	Chip Select 0 and 1. CS0 low and CS1 high selects the CIO.
35	CS1	ZI/O From CPU Sheet 2)	Chip Select 0 and 1. CS0 low and CS1 high selects the CIO.
34	$\overline{AS}$	$\overline{ZAS}$ From CPU (Sheet 2)	Address Strobe. When low, addresses, $\overline{INTACK}$, and $\overline{CS0}$ are sampled. (See Note)
5	$\overline{DS}$	$\overline{ZDS}$ From CPU (Sheet 2)	Data Strobe (active low). Provides timing for data into or out of CIO. (See Note)
16	PCLK	ZCLK From CPU (Sheet 2)	Peripheral Clock. Used to clock the CIO.
25	$\overline{INTACK}$	$\overline{INTA}$ From CPU Status Decoder U23C (Sheet 2)	Interrupt Acknowledge. Indicates to CIO that an interrupt acknowledge cycle is in progress.
24	$\overline{INT}$	$\overline{VI}$ to CPU (Sheet 2)	Vector Interrupt (active low). Requests a CPU vectored interrupt.
17 18	IEI/ IEO	IEI/IEO from Other Daisy-Chained Device	Interrupt Enable In/ Interrupt Enable Out. Control the CIO and CPU interrupt priorities.

Table 6. DMA Control CIO Control Signals

NOTE: $\overline{AS}$ and $\overline{DS}$ low at the same time is an illegal condition and causes the CIO to reset.

SIGNAL	FUNCTION
PCHECK	Received from Cache memory parity checker. Indicates a parity failure in memory. Read/Write Clock to byte counter.
R/W BC	Read/$\overline{\text{Write}}$ clock to byte counter.
IF DOWN, CPU DOWN, R/W DOWN	Sent to Load/$\overline{\text{Run}}$ MUX (Sheet 9) to specify direction of count for DMA address.
IF READ, CPU READ, R/W C READ	Sent to Read/$\overline{\text{Write}}$ MUX (Sheet 9) to specify a read or write operation.
DMA16, DMA 17	High order DMA address bits; sent to bit slicer (Sheet 8) to specify selected CAS to be generated.
FHMPE (Force High Parity Error), FLMPE (Force Low Parity Error), REVERSE BANKS	Used only for diagnostics to force high parity error or low parity error and to change the active (high or low) cache memory bank (REVERSE BANKS).
R/W L BUB (Read/$\overline{\text{Write}}$ Last Byte)	Routed to CIF/Write and Data boards to indicate that the last byte is being read or written.
IF LOAD, CPU LOAD, R/W LOAD	Sent to Load/$\overline{\text{Run}}$ MUX (Sheet 9) to specify a load address or run operation.
CREFRESH	Cache refresh signal; routed to Advance MUX (Sheet 9) to advance the DMA address during a read/write cycle.

Table 7. DMA Control CIO Output Signal Functions

Register Designator	DMA address
R1	LTAPE
R2	CPU
R4	PTAPE

Table 8. DMA Address Register

I 3	I 2/4	CN	OPERATION
0	0	1	Increment B Register
1	0	0	Decrement B Register
1	1	X	Load
X = DON'T CARE			

Table 9. Bit Slice Device Microinstructions

	INCREMENT (I 2/4 - I 3)	DECREMENT (I 2/4 - I 3)	LOAD (I 2/4 - I 3)
ABUF	R2 → Y, INCR R4	RE → Y, DECR R4	RE → Y, LD R4
BBUF	R4 → Y, INCR R1	R4 → Y, DECR R1	R4 → Y, LD R1
CBUF	R1 → Y, INCR R2	R1 → Y, DECR R2	R1 → Y, LD R2

Table 10. Channel Cycles And Bit Slice Device Register Functions

SIGNAL	DESCRIPTION
IGO	Initiate Command. Used to latch the command specified on the command lines into the selected ready GCR.
IFEN	Formatter Enable. Enables the GCR. With GCR on-line and IDBY true, pulse will reset a command "runaway" condition.
IREW	Rewind. Interface input signal. With GCR ready, on-line, and not at BOT, causes tape to rewind in reverse direction.
IRWU	Rewind/Unload. With GCR on-line, causes selected unit to go off line, rewind to BOT marker, then unload the tape.
ILWD	Last Word. Used during a write operation to indicate that the character to be strobed into the formatter is the last character of the record.
IREV IWRT IWFM IEDIT IERASE	Reverse Write Write File Mark Edit Erase Tape drive commands lines. (Decoding these five lines produces the commands shown in Table 3-10).
IWP, IW0-IW7	Write Data. Input lines that carry write data from the host controller to the GCR.
IFAD, ITAD0, ITAD1	Address lines used to select a daisy-chained GCR.

Table 11. Interface Input Signals

COMMAND	IREV	IWRT	IWFM	IEDIT	IERASE
Read Forward	0	0	0	0	0
Read Reverse	1	0	0	0	0
Read Reverse Edit	1	0	0	1	0
Write Forward	0	1	0	0	0
Write Edit	0	1	0	1	0
Write File Mark	0	1	1	0	0
Erase Variable Length	0	1	0	0	1
Erase Fixed Length	0	1	1	0	1
Security Erase	0	1	1	1	1
Space Record Forward	0	0	0	0	1
Space Record Reverse	1	0	0	0	1
Space File Search Forward	0	0	1	0	0
Space File Search Forward (Ignore Data)	0	0	1	0	1
Space File Search Reverse	1	0	1	0	0
Space File Search Reverse (Ignore Data)	1	0	1	0	1
Status Hold	0	0	0	1	1
Select 3200 CPI	1	0	1	1	1
Select 1600 CPI	0	0	1	1	1
Select 6250 CPI	1	1	0	0	0
Read Extended Status	0	0	0	1	0
Diagnostic Write	1	1	1	1	1

Table 12. Tape Drive Input Command Codes

IFAD	ITAD0	ITAD1	LOGICAL ADDRESS
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Table 13. Logical Unit Addresses

SIGNAL	DESCRIPTION
IFBY	Formatter Busy. Indicates that tape motion is occurring.
IDBY	Data Busy. Goes true after simulated ramp delay and remains true during execution of all channels initiated by IGO.
IDENT	Identification. Pulsed when reading or writing from the BOT marker and the PE 3200 or GCR identification burst is detected.
IHER	Hard Error. Pulsed while IDBY is true to indicate that an uncorrectable error has been detected by the GCR. Indicates a machine failure during any write operation other than a write edit; pulsed when add parity sum of IW0-7, IWP is incorrect.
ICER	Correctable Error. During a read/write operation, indicates the occurence of a single-track correctable error.
IFMK	File Mark. Pulsed while IDBY is true to indicate that the GCR has detected a file mark.
IRDY	Ready. Indicates that GCR is on-line, not rewinding, and ready to accept a remote command.
IONL	On-Line. Indicates that selected GCR is accessible to the host controller.
IRWD	Rewinding. Indicates that the tape is rewinding to beginning of tape. IRDY will be false while the tape is rewinding.

Table 14. Interface Output Signals

SIGNAL	DESCRIPTION
IFPT	File Protect. Indicates that a reel of tape without a file protect ring is mounted on a selected GCR.
ILDP	Load Point. Indicates that the BOT marker is positioned in front of the photosensor.
IEOT	End of Tape. Indicates that the EOT marker has been detected.
IWSTR	Write Strobe. Pulsed to indicate that the character on the data lines has been recorded and the next character is needed.
IRSTR	Read Strobe. Pulses to indicate that a character is present on the controller interface.
IRP, IR0-IR7	Read Data. Read data from the GCR to the host controller.

Table 14. Interface Output Signals (Continued)

DATA RATE (kHz)	CONTROL BITS C5	C4	C3	C2	C1
632.8	0	X	X	X	X
316.5	1	1	1	1	0
211.0	1	1	1	0	1
158.2	1	1	1	0	0
126.6	1	1	0	1	1
105.5	1	1	0	1	0
90.4	1	1	0	0	1
79.1	1	1	0	0	0
70.3	1	0	1	1	1

Table 15. Interface Data Transfer Rates And Control Codes

SIGNAL	FUNCTION
	FROM CPU
PLLRESET	Sent to phase lock loop to reset loop.
FWD/REV	Sent to master state machine EPROMs to specifiy direction of tape (forward or reverse).
PE/GCR	Sent to master state machine EPROMs and to pad count logic to specify recording mode selection (PE or GCR).
TERMCNT/TEST	Sent to pad count logic to specify read termination count or test.
WRITE OP	Sent to pad count logic to indicate a write operation in progress.
	TO CPU
STCLKC	Master state machine clock C from Data Board clock generation logic.
PROCINT	Sent from master state machine EPROMs to indicate a processor interrupt.
POSTAM	Sent from master state machine EPROMs to indicate that a postamble has been detected.
BLOCK DET	Sent from block detect logic to indicate that recorded tape has been detected.
CHERR0- CHERR7, CHERRP	Channel error signals sent from individual channel state machines via latches U6B and U6C, also used by CIO U5B to detect ID BURSTS, FILE MARKS and ARA ID BURSTS.
VRERR	Vertical redundancy check error signal sent from cache bus interface logic via latch U6B.

Table 16. Data Board/CPU Status and Control Signals

NOTES: UNLESS OTHERWISE SPECIFIED.

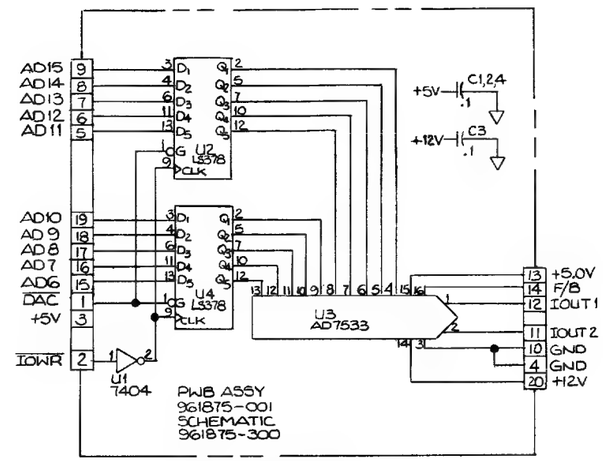
1. RESISTOR VALUES ARE IN OHMS, 1/4W, 5%.
2. CAPACITOR VALUES ARE IN MICROFARADS.
3. IC VOLTAGE AND GND ASSIGNMENTS, UNUSED GATES:

IC TYPE	REFERENCE DESIGNATOR	+5	GND	+12	-12	+6	-6	UNUSED
8251A	U14B	26	4					
ADC1001CCN	U7D	20	10					
DAC1006LCN	U7B	3	11					
LM339	U37.1DL.1IL,19M,14N.19T		12	3				U11L-B
MC1405B1P	U4E.5E,7G		8			16	7	
MC3488AP	U12L		4	8	5			
SN74LS11N	U12N, 19V	14	7					U12N-A,19V-A
RC4136	U9N. 15K,17K, 19P, 19S			11	7			U19S-A.B. U17K-A B.D
SN7414N	U16J	14	7					U16J-E
SN7407N	U9G, U17V	14	7					U9G-A.B.C, U17V-E, F
SN74LS08N	U12G. 13G, 15H	14	7					U15H -A
SN74LS123N	U14H	16	8					
SN74LS00N	U17H	14	7					U17H-A,B
SN74LS138N	U15E	16	8					
SN74LS14N	U12H. 15G	14	7					U15G-A,B,D,E,F
SN74LS175	U15B, 17E	16	8					
SN74LS32N	U16G	14	7					U16G-A,B
SN74LS74N	U15J	14	7					
TL082P	U6B,6C,6D,6E,6F			8	4			U6B-A
UA555TC	U4V	8	1					
UC3524AN	U3V		8					
Z8036APS	U10B, U12B	23	7					
SN74LS10N	U17G	14	7					U17G-A,B
SN74LS04N	U16E	14	7					C,D,E,F
SN74LS244N	U17B	20	10					H
MC7406P	U9E	14	7					9E-D,E

4. LAST USED AND UNUSED REFERENCE DESIGNATORS:

REFERENCE DESIGNATION		
LTR	LAST USED	NOT USED
C	165	
CR	49	
DS	1	
L	9	
Q	30	
R	337	
T	1	
TP	45	
VR	6	
K	1	

5 ALTERNATE SCHEM SECTION (DETAIL A) TO BE USED WITH PWB ASSY 961344-001.

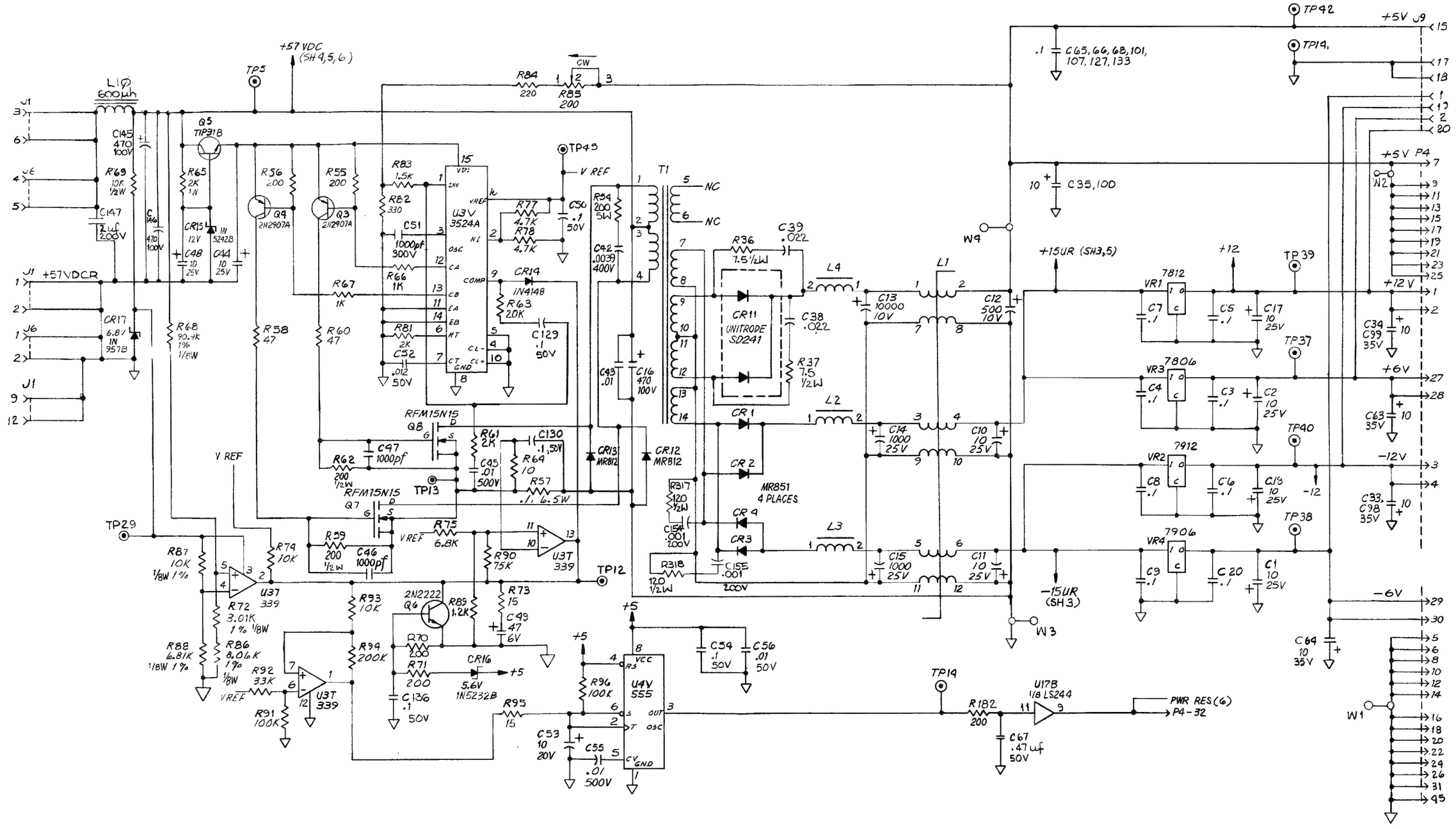


5 DETAIL A
SEE SHEET 4

SENSE/SERVO BOARD

Schematic No. 1

Sht 1 of 7



SENSE/SERVO BOARD

Schematic No. 1

Sht 2 of 7

ERASE HEAD DRIVER

EARLY ERASE HEAD DRIVER

WRITE CENTER TAP HEAD DRIVER

SENSE/SERVO BOARD

Schematic No. 1

SENSE/SERVO BOARD

Schematic No. 1

Sht 4 of 7

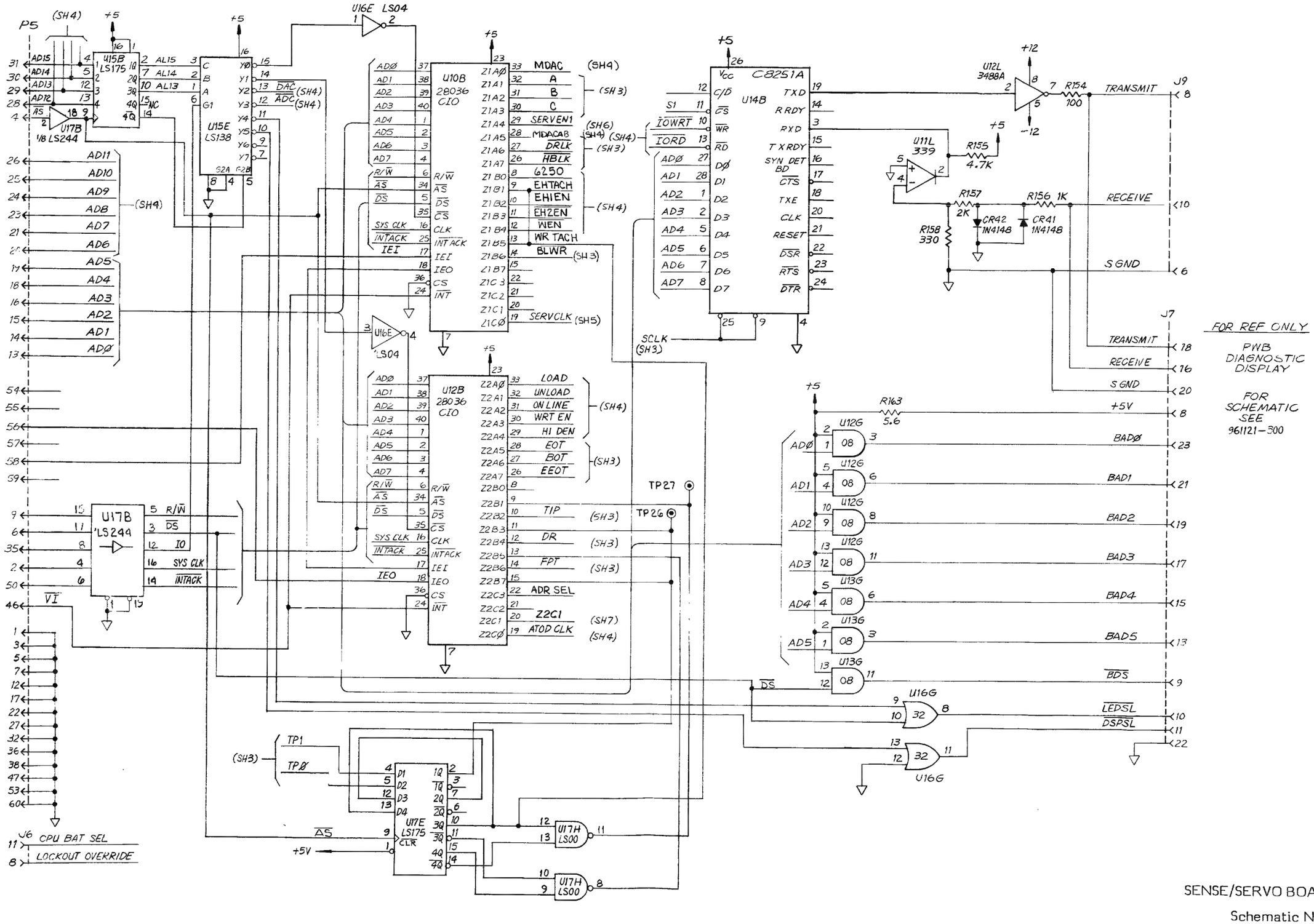
SUPPLY SERVO

SENSE/SERVO BOARD

Schematic No. 1

Sht 5 of 7

K1-6 TUD (SH 5)
K1-7 TUDD (SH 5)
+57VDC (SH2)
+12V
+5V
-12V
TP3
TP9
TP30
TP31
TP32
TP36
TP41
TP43
SH5
TMV (SH4)
TMI (SH4)
ITU (SH4)
Z2C1 (SH7)
P5-43 WATCHDOG ENABLE
+5VREG(SH5)
PWR RES (SH2)
SERV EN 1 (SH7)
SERV EN 2 (SH5)
DS1 FAILURE
REF
B2
TAKE UP MOTOR
TUDR
POWER DETECTION CIRCUIT
TAKE UP SERVO
HII
f+
f-
FWD
REV
7407N
SNT4LS11N
SENSE/SERVO BOARD
Schematic No. 1
Sht 6 of 7



SENSE/SERVO BOARD

Schematic No. 1

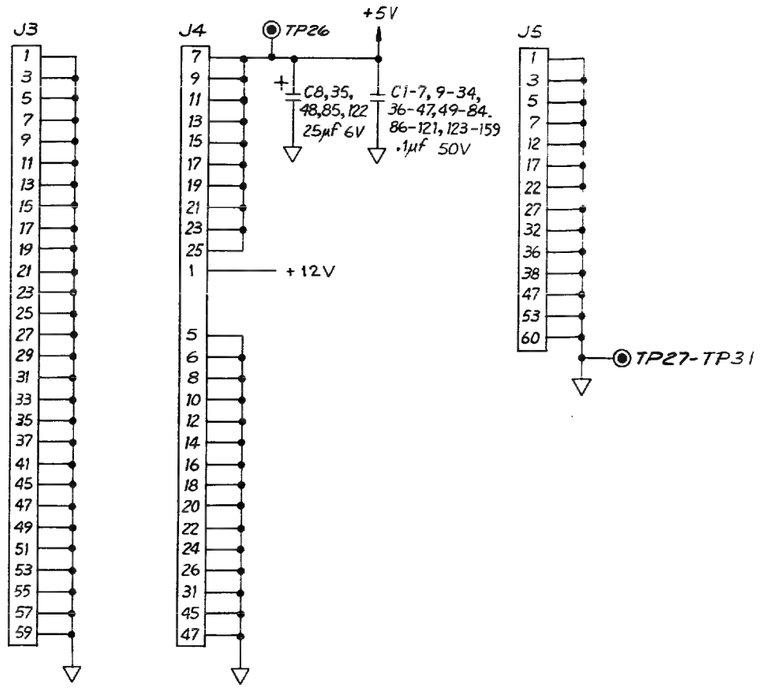
Sht 7 of 7

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. IC V_{CC} & GND PINS WITH UNUSED PORTIONS:

IC TYPE	REFERENCE DESIGNATOR		+5V	GND	UNUSED
SN74LS00N	16N, 18H, 22C, 25D		14	7	
SN74LS01N	23H		14	7	C
SN74LS04N	23B		14	7	
SN74LS08N	22D, 27H		14	7	27H-D
SN74LS10N	18A		14	7	
SN74LS11N	14C		14	7	C
SN74LS14N	3C		14	7	E, F
SN74LS28N	22H		14	7	
SN74LS32N	17C, 20C, 20J, 25H		14	7	
SN74LS42N	23C		16	8	
SN74LS74N	15L, 16D, 16L, 17F, 18C, 22B		14	7	22B-A
SN74LS109N	20B		16	8	
SN74LS125N	20H		14	7	
SN74LS138N	27J		16	8	
SN74LS139N	27D		16	8	
SN74LS153N	17H, 18D, 18F		16	8	
SN74LS244N	3A, 6C, 9A, 9B, 12C, 16B, 22A, 27A		20	10	16B-A 3A-G, 27A-C, E, G
SN74LS245N	23A, 25A		20	10	
SN74LS256N	14J		16	8	
SN74LS280N	22J, 23J		14	7	
SN74LS374N	17K, 17L		20	10	
74S112PC	16J		16	8	
DM74S135N	18J		16	8	
74S280N	6B, 9C		14	7	
74F32	U16A		14	7	U16A-B, C, D
74F00PC	15H		14	7	
74F04PC	17J		14	7	
74F08PC	3B		14	7	B, C, D
74F74PC	12B, 15K, 16K, 17D, 23D		14	7	15K-B
74F86PC	14B		14	7	
74F109PC	15C, 16C		16	8	15C-B
74F138PC	16H		16	8	
74F191PC	16F		16	8	
74F373PC	22F, 27F		20	10	
74F374PC	6A, 6J, 9J		20	10	
27128	20K, 22K, 23K, 25K,		28	14	
AM2901CPC	3K, 6K, 9K, 12K, 14K		10	30	
AM2947PC	23F, 25F		20	10	
AM2966PC	3J 12J 15D 15F 18M 27M 27P		20	10	15D-A, C, E, G
M5K4164ANP-15	1D, 2D, 4D, 5D, 7D, 8D, 10D, 11D, 13D, 14D, 1E, 2E, 4E, 5E, 7E, 8E, 10E, 11E, 13E, 14E, 1G, 2G, 4G, 5G, 7G, 8G, 10G, 11G, 13G, 14G, 1H, 2H, 4H, 5H, 7H, 8H, 10H, 11H, 13H, 14H, 19M, 21M, 22M, 23M, 24M, 26M, 19N, 21N, 22N, 23N, 24N, 26N, 19P, 21P, 22P, 23P, 24P, 26P		8	16	
X2210D	25J		18	8	
Z8002APS	25B		10	31	
Z8036APS	20D		23	7	
Z8581PS	27C		5	14	
LM3911N	14N		-	1	
898-5-R220/330	12A (RESISTOR NETWORK)		16	8	PINS 5,6,7,14

2. POWER & GND ON CONNECTORS:



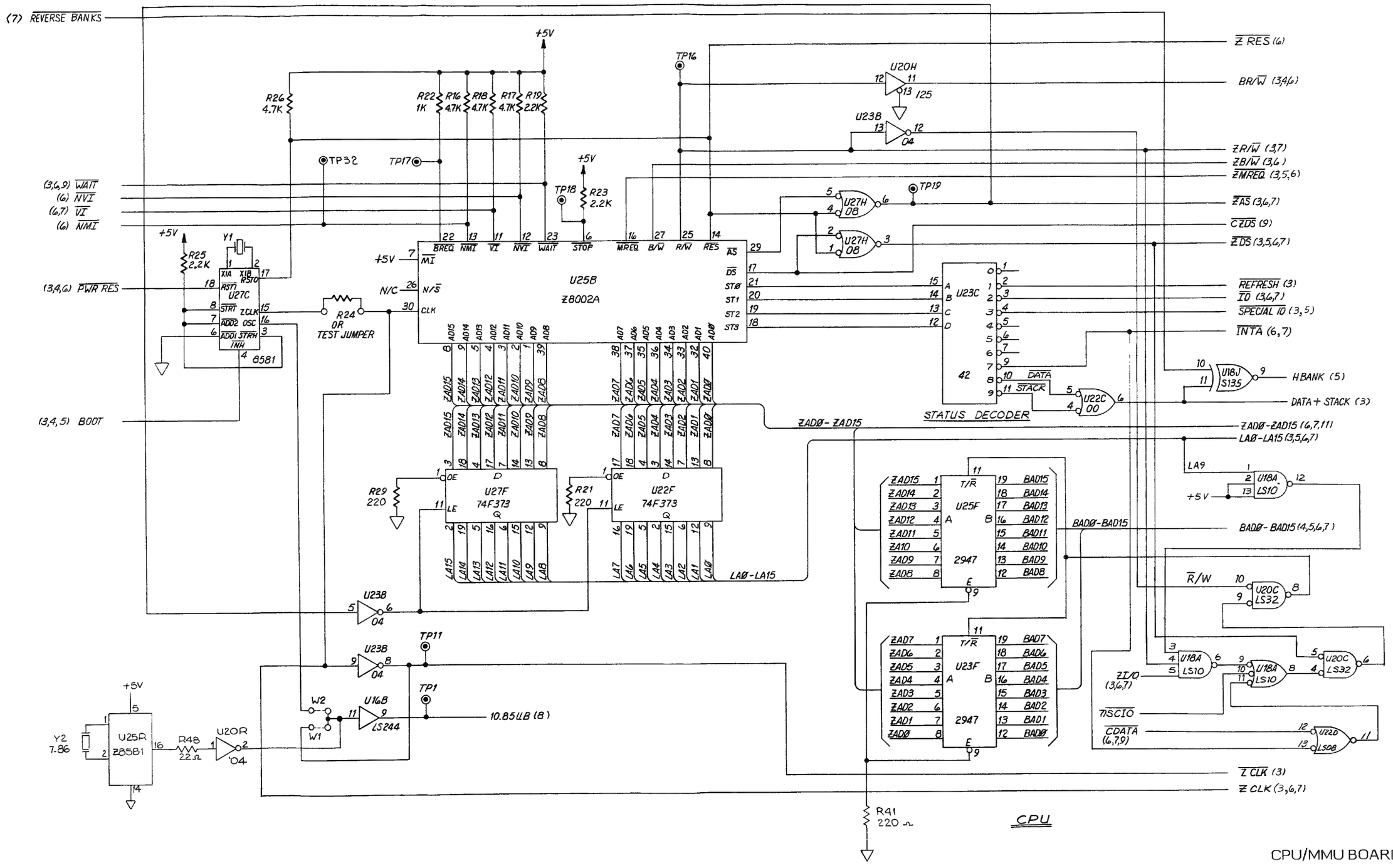
3.

REFERENCE DESIGNATOR					
LTR	LAST USED	NOT USED	LTR	LAST USED	NOT USED
C	161		TP	34	13, 14, 21
CR	1		Y	1	
P	5	1, 2	U	27P	
Q	2				
R	47	27, 28, 32, 40			

4. RESISTOR VALUES ARE IN OHMS, ¼ W, 5%

CPU/MMU BOARD

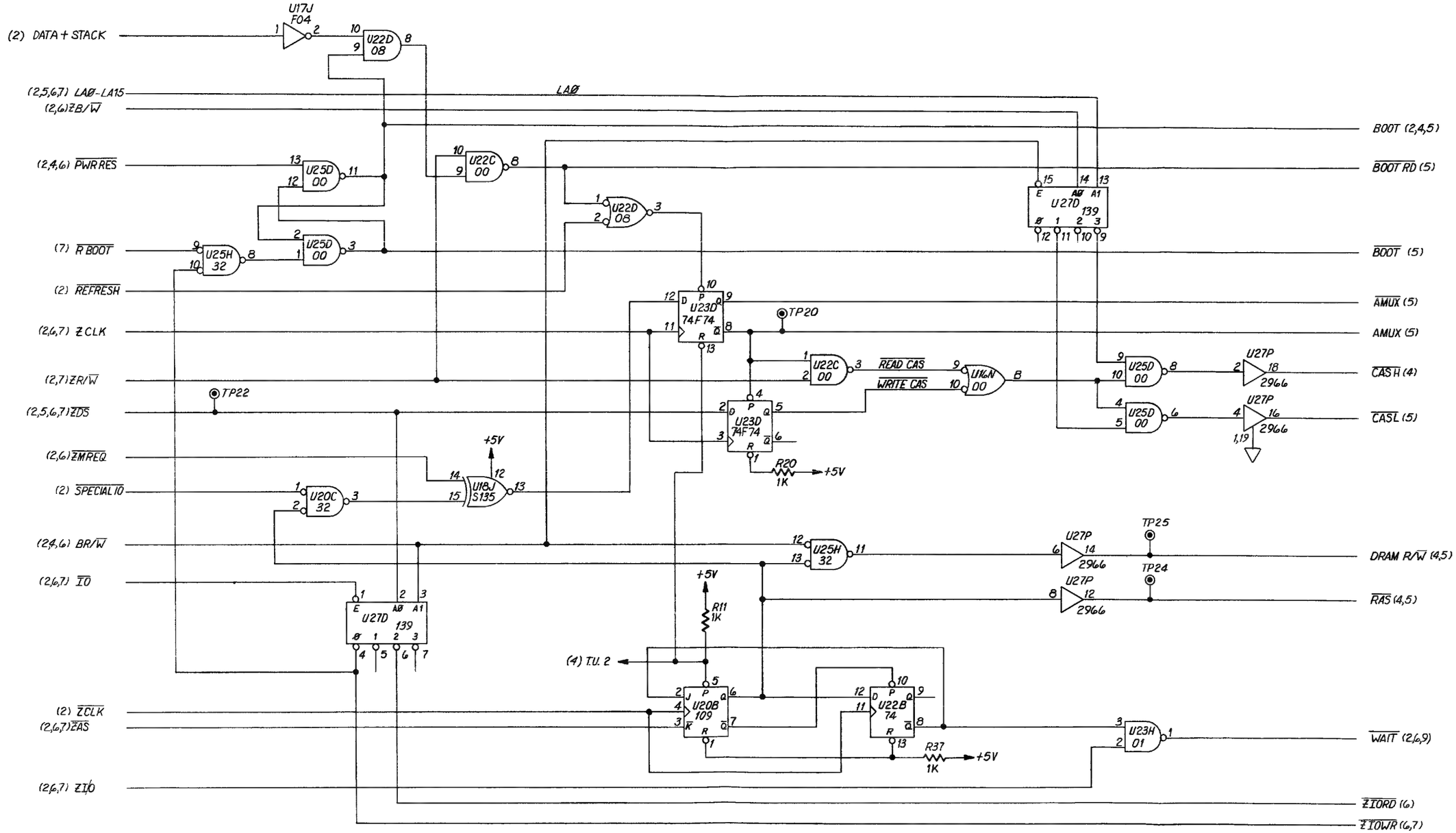
Schematic No. 2



CPU/MMU BOARD

Schematic No. 2

Sht 2 of 11



CPU DRAM / BOOT CONTROL

HIGH BYTE

(3,5) $\overline{RAS}$
(3,5) DRAM R/$\overline{W}$
(3) $\overline{CASH}$
(5) A0-A7
(2,5,6,7) BAD0-BAD15
(2,3,6) BR/$\overline{W}$
(7) FHMPE
(5) RPL
(7) FLMPE
(5) $\overline{RAM\ DS}$
(2,3,5) BOOT
(2,3,6) $\overline{PWR\ RES}$

U23M 4164 — RPH
U26M 4164 — BAD15
U26P 4164 — BAD14
U26N 4164 — BAD13
U24M 4164 — BAD12
U24N 4164 — BAD11
U23P 4164 — BAD10
U23N 4164 — BAD9
U24P 4164 — BAD8
+5V
A0-A7
BAD0 - BAD15

J5: 1, 3, 5, 7, 12, 17, 22, 27, 32, 36, 38, 47, 53, 60

BAD8-BAD15
U23J LS280 (BAD10, BAD11, BAD12, BAD13, BAD14, BAD15, BAD8, BAD9)
RPH
U18H 00
U18J S135
U20H 125 RPH
BAD0-BAD7
U22J LS280 (BAD2, BAD3, BAD4, BAD5, BAD6, BAD7, BAD0, BAD1)
+5V
U18H 00
U18J S135
U20H 125 RPL
H PARITY
L PARITY
U20J 32 — P ERROR
T.U.2 (3)
U20B 109
TP12
WDOG ENA UB (6)
U22H 28
U18H 00
PARITY / DRAM HIGH

CPU/MMU BOARD
Schematic No. 2
Sht 4 of 11

LOW BYTE

(4) RPL
(2,4,6,7) BAD0-BAD15
(3,4) RAS
(3,4) DRAM R/W
(3) CASL
BAD0-BAD15
A0-A7
+5V
A0-A7 (4)

U19M 64K 4164 PL — RPL
U19N 4164 — BAD7
U19P 4164 — BAD6
U21M 4164 — BAD5
U21N 4164 — BAD4

DRAM ADDRESS MUX/BUFFER

(2) HBANK
(2,3,6,7) LA1-LA15
(3) AMUX

U18M 2966

U21P 4164 — BAD3
U22M 4164 — BAD2
U22N 4164 — BAD1
U22P 4164 — BAD0

LA1-LA15
BAD0-BAD15

U27M 2966

U20K 27128
U23K 27128
U22K 27128
U25K 27128

LA15
(2,3,4) BOOT
(3) BOOT
(3) BOOT RD
(2,3,6,7) ZDS
(2) SPECIAL IO
(2) ZMREQ

U18H 00
U20J 32
U22D 08
U20J 32
U20J 32

RAMDS (4)

EPROM / DRAM LOW

CPU/MMU BOARD
Schematic No. 2

J5 IN

42 WAIT (2,3,9)
46 VI (2,7)
48 NVI (2)
49 NMI (2)
54 E8 INTØ
55 E7 INT1
56 E6 INT2
57 E5 INT3
58 E4 INT4
59 E3 INT5

U17J F04

U116N LS00

U14C LS11

U14B F86

IEO E1 IEO (7)
IEI E2 IEI (7)

ZADØ - ZAD7

ZAD8 - ZAD15

U22H 28

U23B 04

U25A 245
U23A 245
B A
G T/R

ZADØ 11
ZAD1 12
ZAD2 13
ZAD3 14
ZAD4 15
ZAD5 16
ZAD6 17
ZAD7 18
ZAD8 11
ZAD9 18
ZAD10 17
ZAD11 16
ZAD12 15
ZAD13 14
ZAD14 12
ZAD15 13

J5 OUT

13 ADØ
14 AD1
15 AD2
16 AD3
18 AD4
19 AD5
20 AD6
21 AD7
23 AD8
24 AD9
25 AD10
26 AD11
28 AD12
29 AD13
30 AD14
31 AD15

J4

+5V C8,35,48,85,122 25µfd + C1-7, 9-14, 36-47, 49-84, 86-121, 123-159 .1

(7) +12V

(11) PRTERM

TP33

32 PWR RES

(2,3,7) IO
(2,7,11) ZADØ-ZAD15
(2,3,5,7) LA9
(2,3,7) ZCLK
(2,3) ZAS
(2,3,5,7) ZDS
(2,3) ZMREQ

U27A 244
OE OE

2 SYS CLK
4 AS
6 DS
8 MREQ
9 R/W

U14B F86

U3C LS14

(2,3) ZB/W
(4) WDOG ENA UB
(2) Z RES
(2,7) INTA

U22A 244

37 B/W
43 WATCHDOG ENABLE
45 RESET
50 INT ACK
33 IOWR
34 IORD
35 IO

U22C LS00

PWR RES (2,3,4)
ENA (7)
ZI/O (2,3,7)
RD CDATA (11)

+5V

R15 1K
TP15
U23B 04

R30 2.2K

(7,9) C DATA

U20C 32

(2,3,5,7) LA0-LA15
(7) STORE NP
(3,7) ZIOWR
(2,3,4) BR/W
(7) RECALL NR
(3) ZIORD

LA1- LA6

U22H 28
U23H 01
U25H 32
U27H 08

(7) SNRM

U25H 32

U25J 2210 NOVRAM

LA1 LA2 LA3 LA4 LA5 LA6
A0 A1 A2 A3 A4 A5
STORE RECALL WE CS
I/O I/O I/O I/O

12 BAD0
13 BAD1
14 BAD2
15 BAD3

BAD0-BAD3

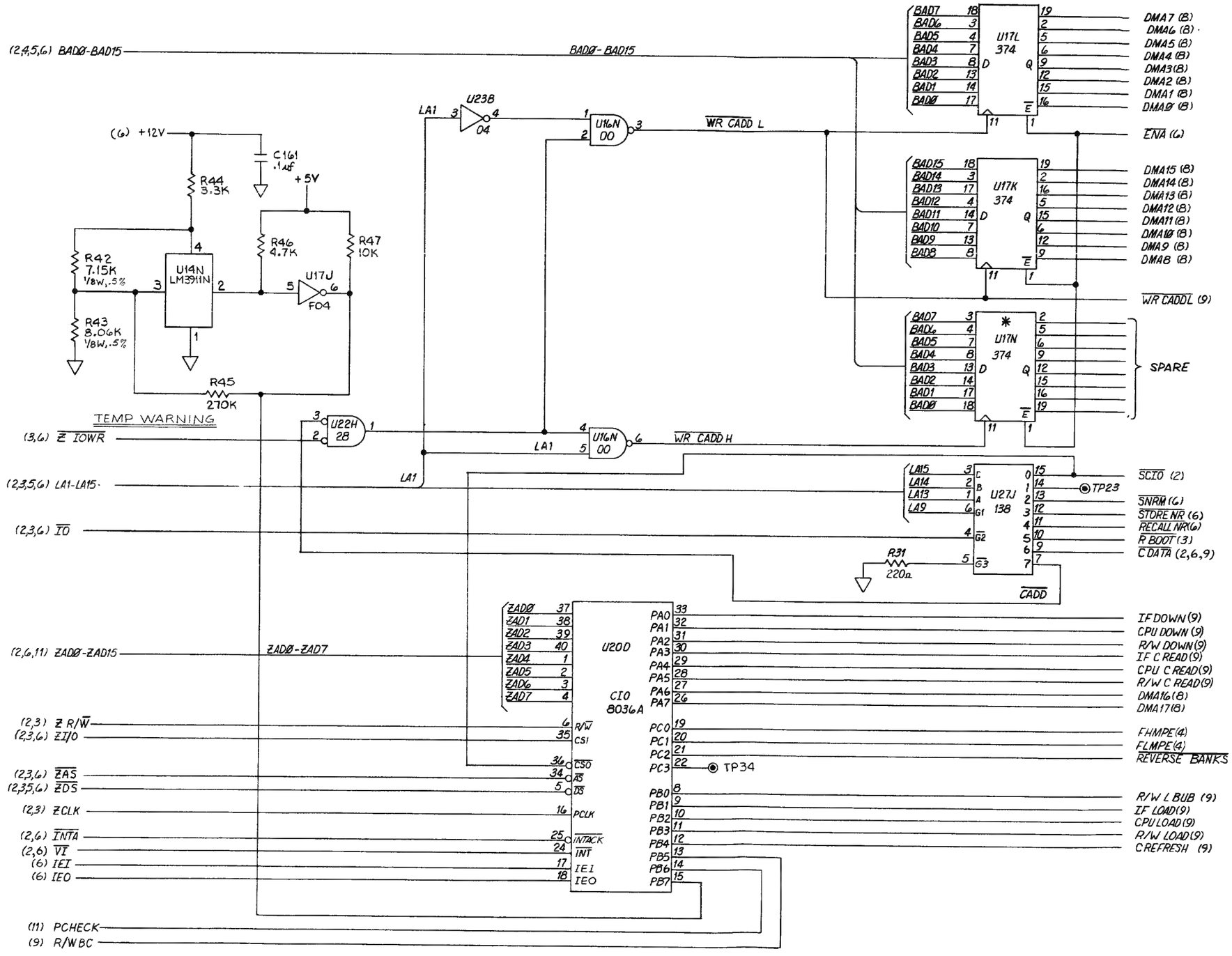
BAD0-BAD15 (2,4,5,7)

+5V

CR1 1N5228B 3.9V,5%
R34 30
R33 100
Q1 2N4401
R35 10K
Q2 2N4401
R36 2.2K

J4/J5/NOVRAM

CPU/MMU BOARD
Schematic No. 2

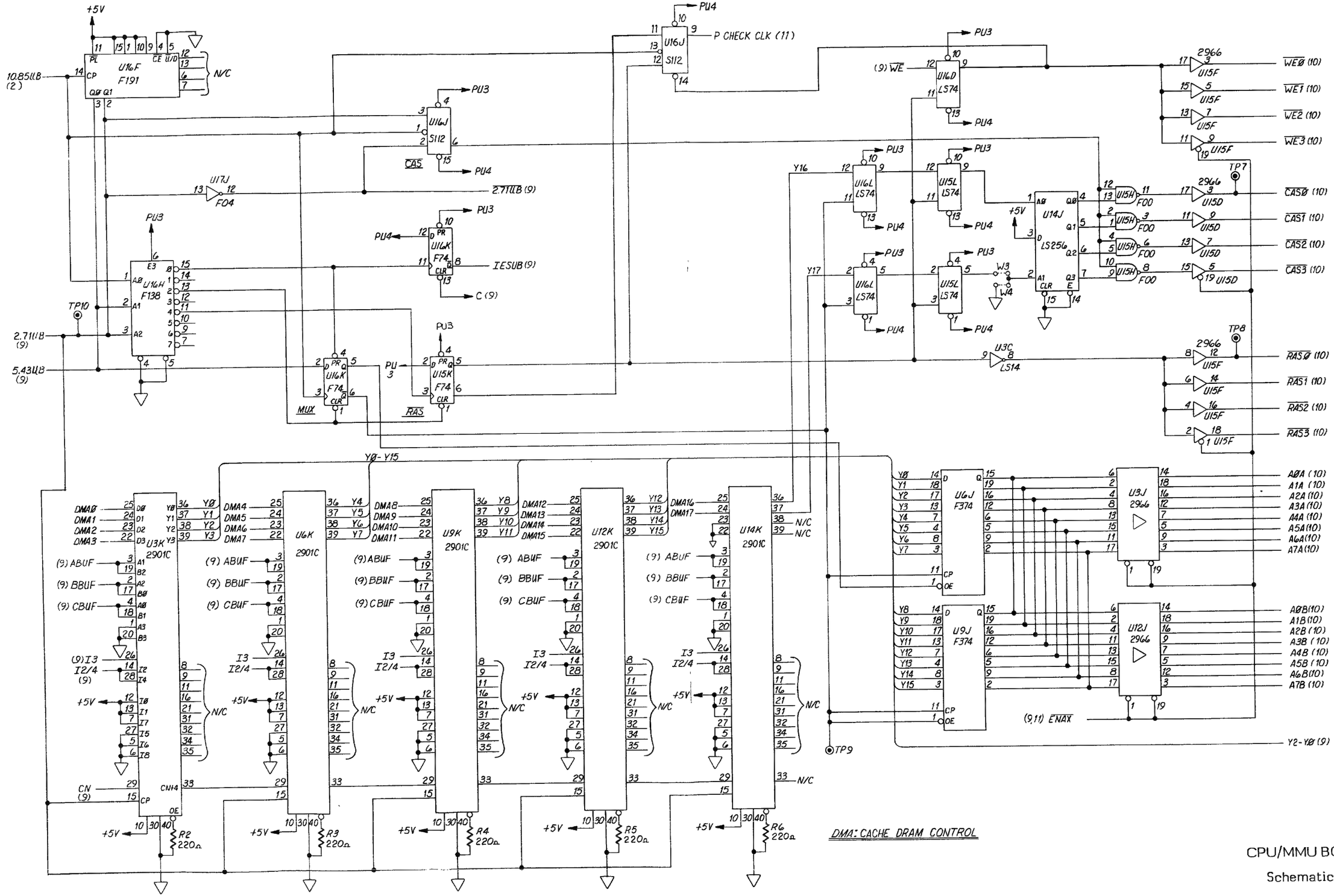


* NOTE: THIS I.C. NOT INSTALLED

TEMP WARNING / DMA CONTROL

CPU/MMU BOARD

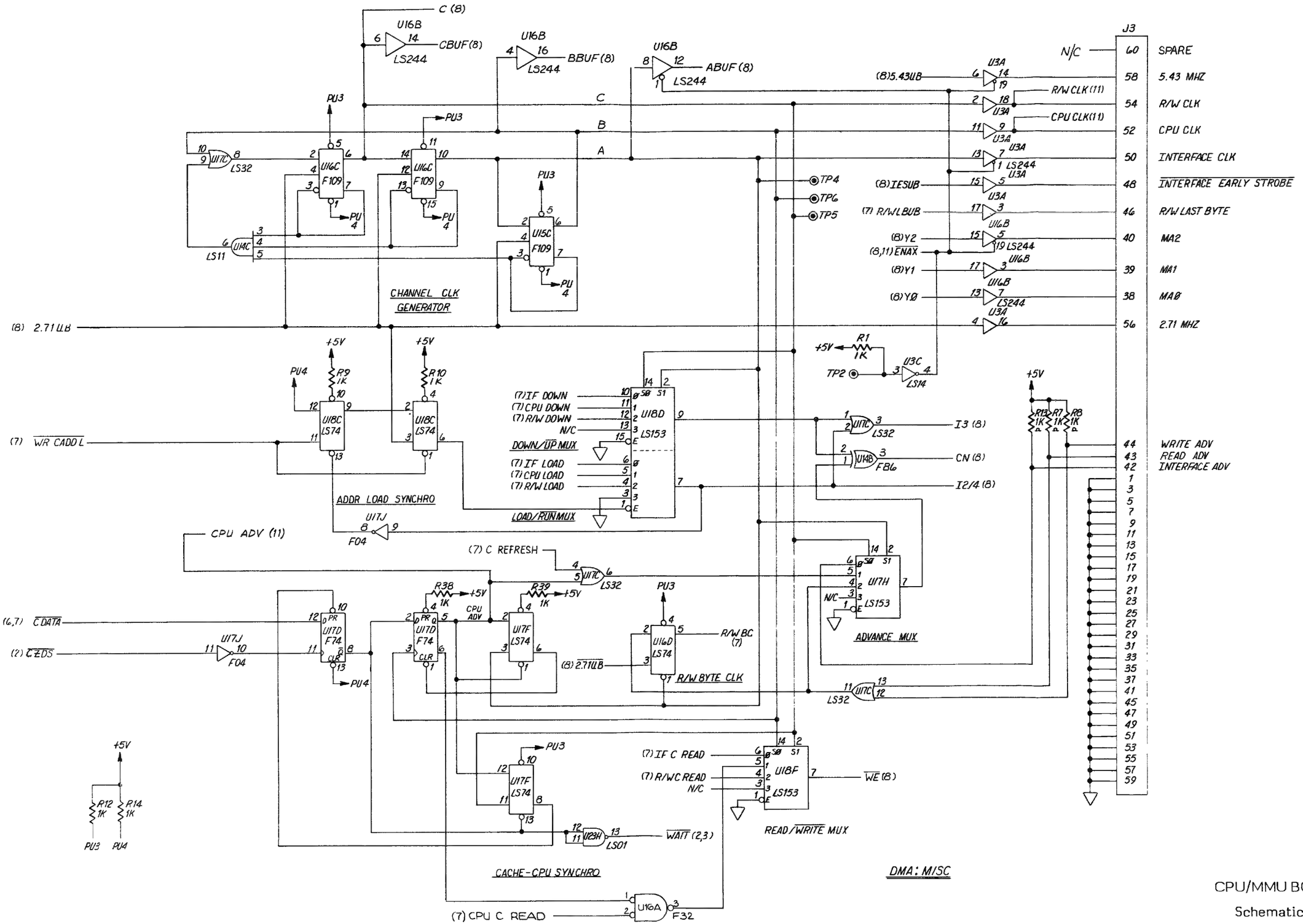
Schematic No. 2



DMA: CACHE DRAM CONTROL

CPU/MMU BOARD

Schematic No. 2



CPU/MMU BOARD

Schematic No. 2

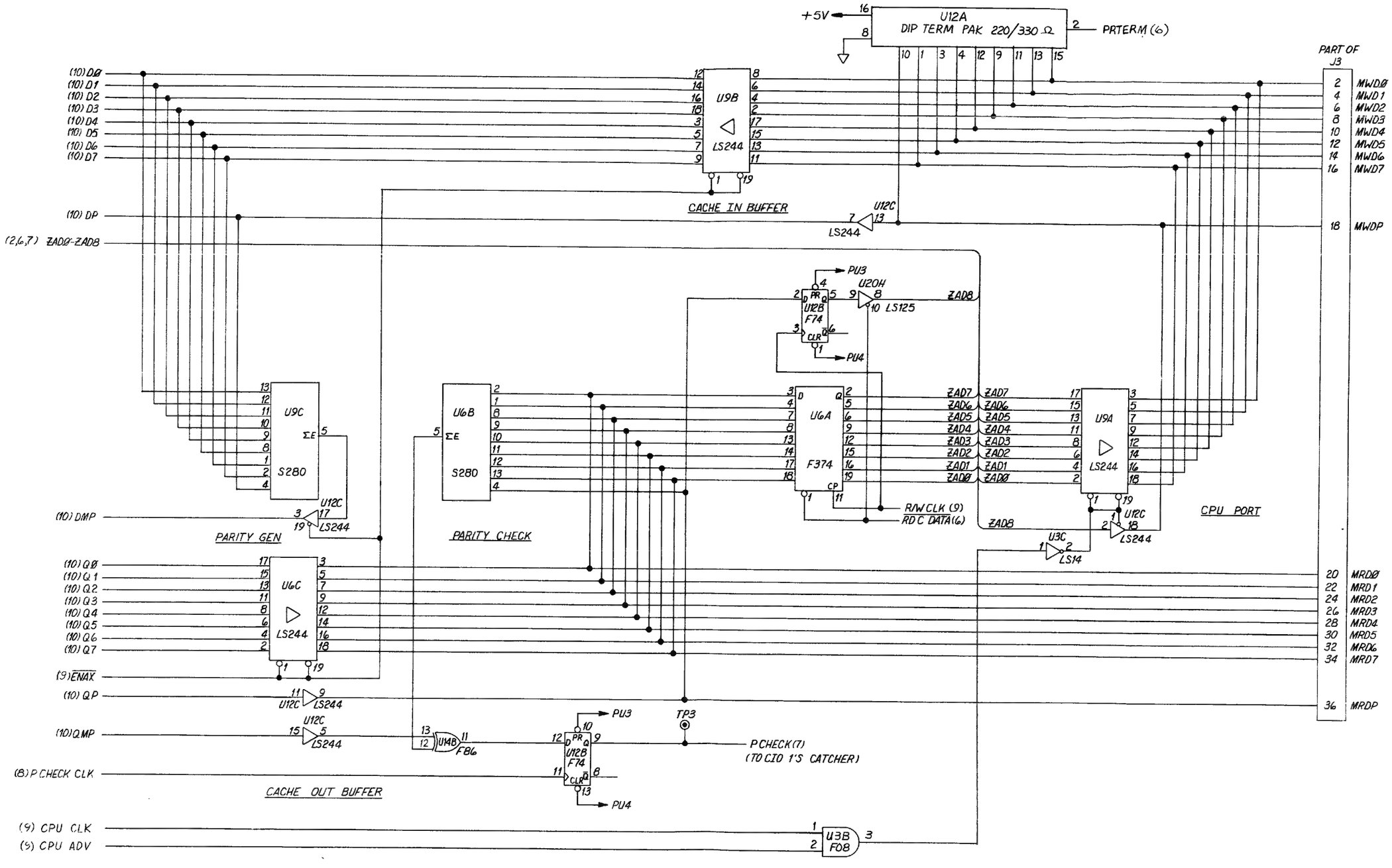
NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DEVICES, SIGNALS, AND PIN NUMBERS, IN THIS SERIES, ARE IDENTICAL.

DMA: CACHE DRAM

CPU/MMU BOARD

Schematic No. 2

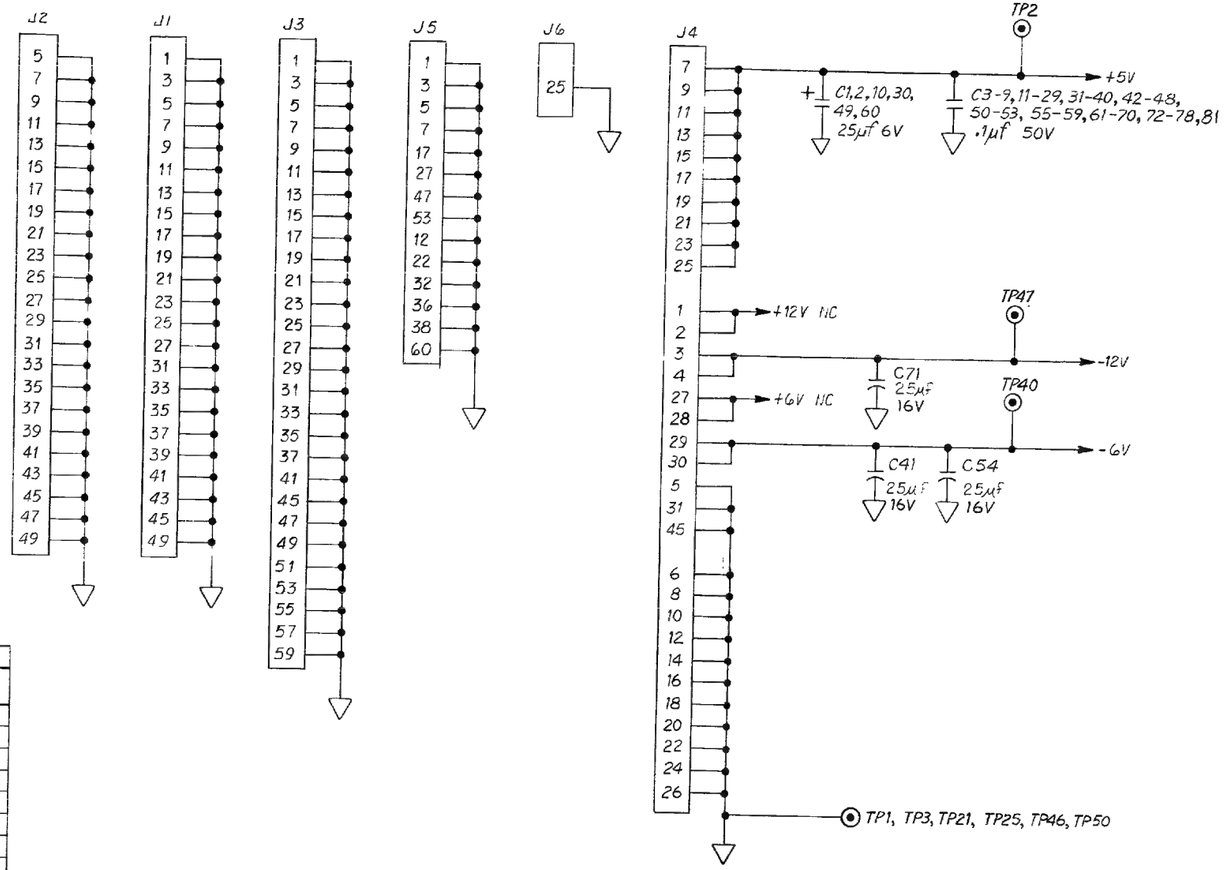


CPU/MMU BOARD

Schematic No. 2

Sht 11 of 11

I.C. TYPE	REFERENCE DESIGNATOR	+5V	-12V	GND	UNUSED
74LS00	7H, 12H, 8J, 10L, 8M	14		7	
74LS02	11H	14		7	11H-C
74LS04	9J, 4L, 5L, 5P, 10K	14		7	5P-A Or-A,C,D
74LS08	8H, 6J, 7J, 6L, 6M, 10M, 10N, 3P, 7P, 5K	14		7	5K-D
74LS10	5J, 9K, 8P	14		7	
74LS11	8K, 7L, 9M, 8N, 9P	14		7	
74LS14	3L	14		7	3L-A,B,C,D,E
74LS32	7K, 7M, 11M, 4N, 5N, 10J	14		7	
74LS38	12C	14		7	13C-A,B,D
74LS74	4K, 6K, 5L, 8L, 11L, 4M, 5M, 7N, 6P	14		7	1F-B, 4K-A
74LS86	15F, 5H, 15L, 13P	14		7	15F-A, 13P-B
74LS123	14P	16		8	
74LS125	2F, 11J, 2P	14		7	11J-D, 2P-D
74LS138	9H, 10H	16		8	
74LS161A	4H, 4J, 13J	16		8	
74LS244	1D, 15D, 4E, 3F, 4F, 2L, 12P, 13R, 1L	20		10	
74LS245	14E, 14F	20		10	
74LS280	12D, 3E	14		7	
74LS368	6H	16		8	
74LS373	12E, 13E, 15E, 9F, 10F, 11F, 12F	20		10	
74LS374	1N, 2N, 3N, 5E, 8E	20		10	
74F04	11K	14		7	11K-B,C,D,E,F
74F08	11P	14		7	11P- B
74F10	11N, 10P	14		7	11N-A,
74F11	12J	14		7	12J-A
74F32	6N	14		7	6N-A,C
74F74	1F, 4P	14		1	4P-A
74F240	1H	20		10	
74F244	2E, 7E	20		10	
74F374	1E, 1J, , 3J, 3R	20		10	
7414	4D, 5D, 6D, 7D, 8D	14		7	
7438	9D, 10D, 11D, 9E, 10E, 11E	14		7	
7474	15H, 15J, 13K, 15K, 13L, 13M, 15M, 13N, 15N	14		7	
2732A	1M, 2M, 3M	24		12	
825159	4R, 5R, 6R, 7R, 8R, 9R, 10R, 11R, 12R	20		10	
LM339	15P	3	12		15P-A,C,D
Z8036A	13F	23		7	
PAL20X8	5F	24		12	
PAL20X10	6F, 7F	24		12	
6349-2	1K, 2K, 3K	20		10	
74S374	2J	20		10	



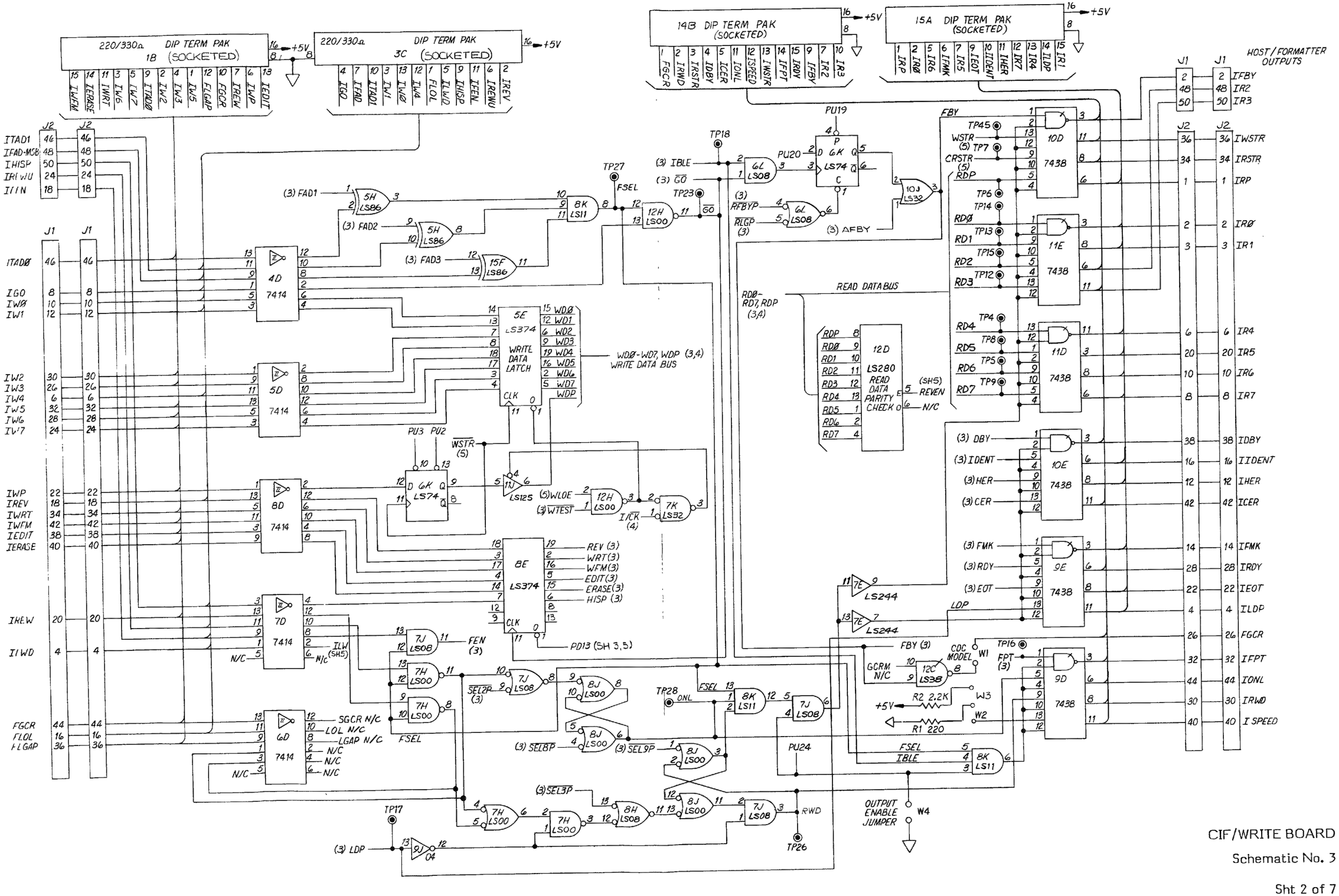
REFERENCE DESIGNATIONS					
LTR	LAST USED	NOT USED	LTR	LAST USED	NOT USED
C	82		S		
CR	901		TP	65	
DS			U	15P	
J	6	1,2	VR		
K			Y		
L			W	4	
P	2		E		
Q	1, 902				
R	27, 909				

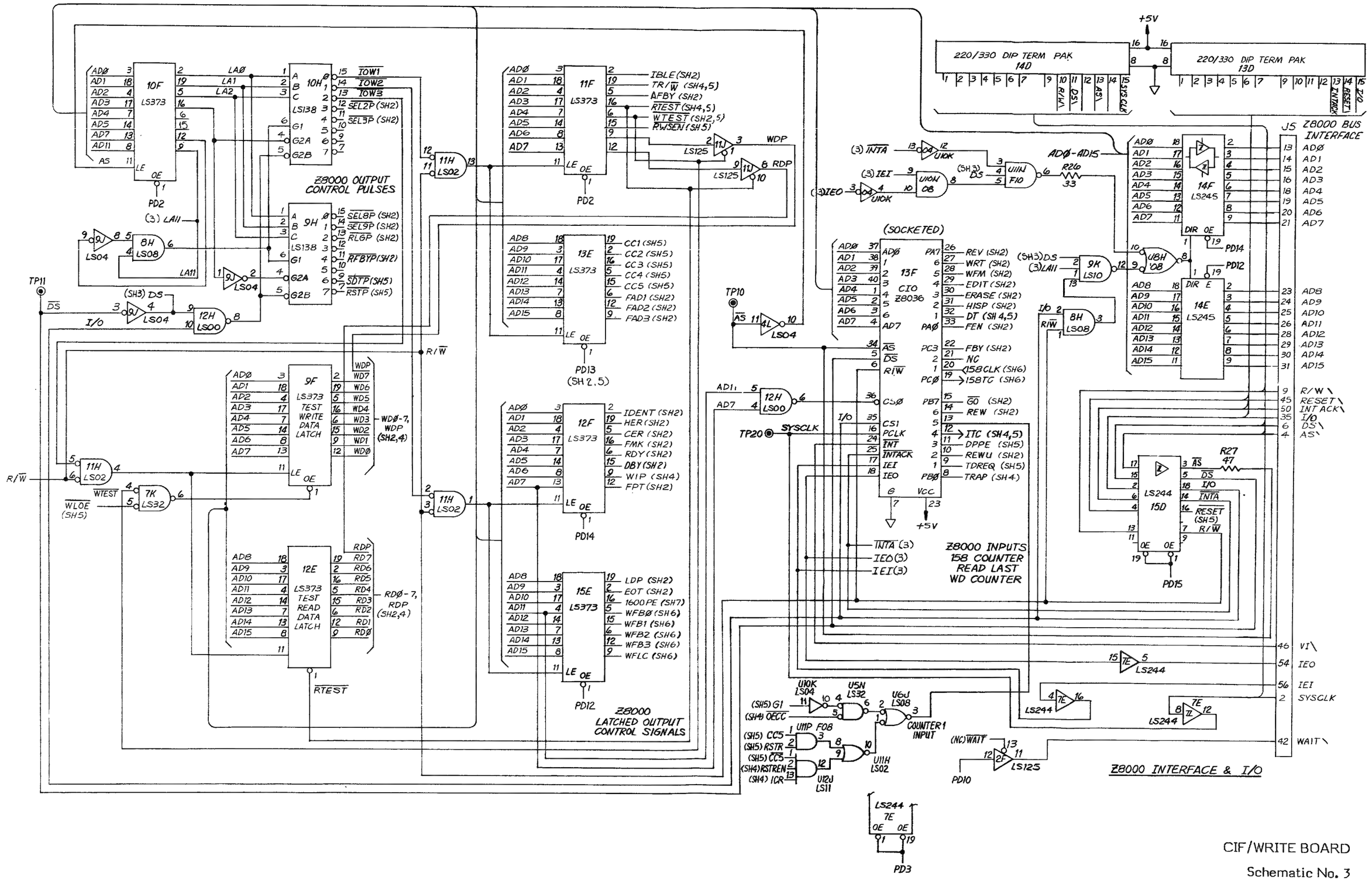
3. VALUES FOR RX05, RX06 DIFFER AMONG M990 & M991.
   SEE PARTS LIST 961346-001 FOR CORRECT VALUES FOR M991.
2. CAPACITOR VALUES ARE IN MICROFARADS.
1. RESISTOR VALUES ARE IN OHMS, 1/4W, 5%.

NOTES: UNLESS OTHERWISE SPECIFIED

CIF/WRITE BOARD

Schematic No. 3


220/330Ω DIP TERM PAK 1B (SOCKETED)
220/330Ω DIP TERM PAK 3C (SOCKETED)
14B DIP TERM PAK (SOCKETED)
15A DIP TERM PAK (SOCKETED)
+5V
IWEN IERASE IWRT IWS IW7 IW2 IW3 IW4 IW5 FLGAP FGCR IREW IWP IEDIT
IGO IFAD IIAD1 IW1 IW0 IW4 FLOL ILWD IHISP IEEN IREWU IREV
FGCR IRWD IRSTR IDBY ICER IONL IWSPEED IWSTR IFPT IRDY IFBY IR2 IR3
IRP IRØ IR6 IFMK IR5 IEOT IHER IR7 IR4 ILDP IR1
HOST/FORMATTER OUTPUTS
ITAD1 IFAD-MSB IHISP IRI WU I/IN
ITADØ IGO IWØ IW1 IW2 IW3 IW4 IW5 IW6 IW7
IWP IREV IWRT IWFM IEDIT IERASE
IHEW IIWD
FGCR FLOL FLGAP
(3) FAD1 (3) FAD2 (3) FAD3
(3) IBLE (3) GO (3) RFBYP (3) RLDP (3) AFBY
FSEL TP18 TP23 TP27 TP28 TP45 TP6 TP14 TP13 TP15 TP12 TP4 TP8 TP5 TP9 TP16
WSTR (5) CRSTR (5) RDP RDØ RD1 RD2 RD3 RD4 RD5 RD6 RD7
RDØ-RD7, RDP (3,4)
READ DATA BUS
WDØ-WD7, WDP (3,4) WRITE DATA BUS
WRITE DATA LATCH
READ DATA PARITY CHECK
(SH5) REVEN N/C
(3) DBY (3) IDENT (3) HER (3) CER (3) FMK (3) RDY (3) EOT
LDP
FBY (3)
GCRM N/C
COC MODEL
+5V R2 2.2K R1 220 W1 W2 W3
PU19 PU20 PU24 PU2 PU3
WLOE (5) WTEST (3) ICK (4)
REV (3) WRT (3) WFM (3) EDIT (3) ERASE (3) HISP (3)
PD13 (SH 3,5)
FEN (3) ILW (SH5)
SEL2P (3) SEL8P (3) SEL9P (3) SEL3P (3)
SGCR N/C LOL N/C LGAP N/C
OUTPUT ENABLE JUMPER W4
RWD TP26 TP17 (3) LDP
CIF/WRITE BOARD
Schematic No. 3
Sht 2 of 7



CIF/WRITE BOARD

Schematic No. 3

Sht 3 of 7

RESIDUAL COUNTERS

CIF CONTROL STATE MACHINE

STATE MACHINE EAC & CACHE INTERFACE

DMA/CACHE MEMORY INTERFACE

WDØ-WD7, WDP

CIF/WRITE BOARD

Schematic No. 3

REDUCED RATE COUNTER

EAC LOGIC CLOCKS

CIF WRITE STROBE

CIF READ STROBE

INTERFACE DATA TRANSMISSION

DMA ADDRESS ADV/ HOLD

WRITE REDUCED RATE

READ REDUCED RATE

STATE MACHINE CLOCK

R OR W MAX RATE

WRITE DATA LATCH OUTPUT ENABLE

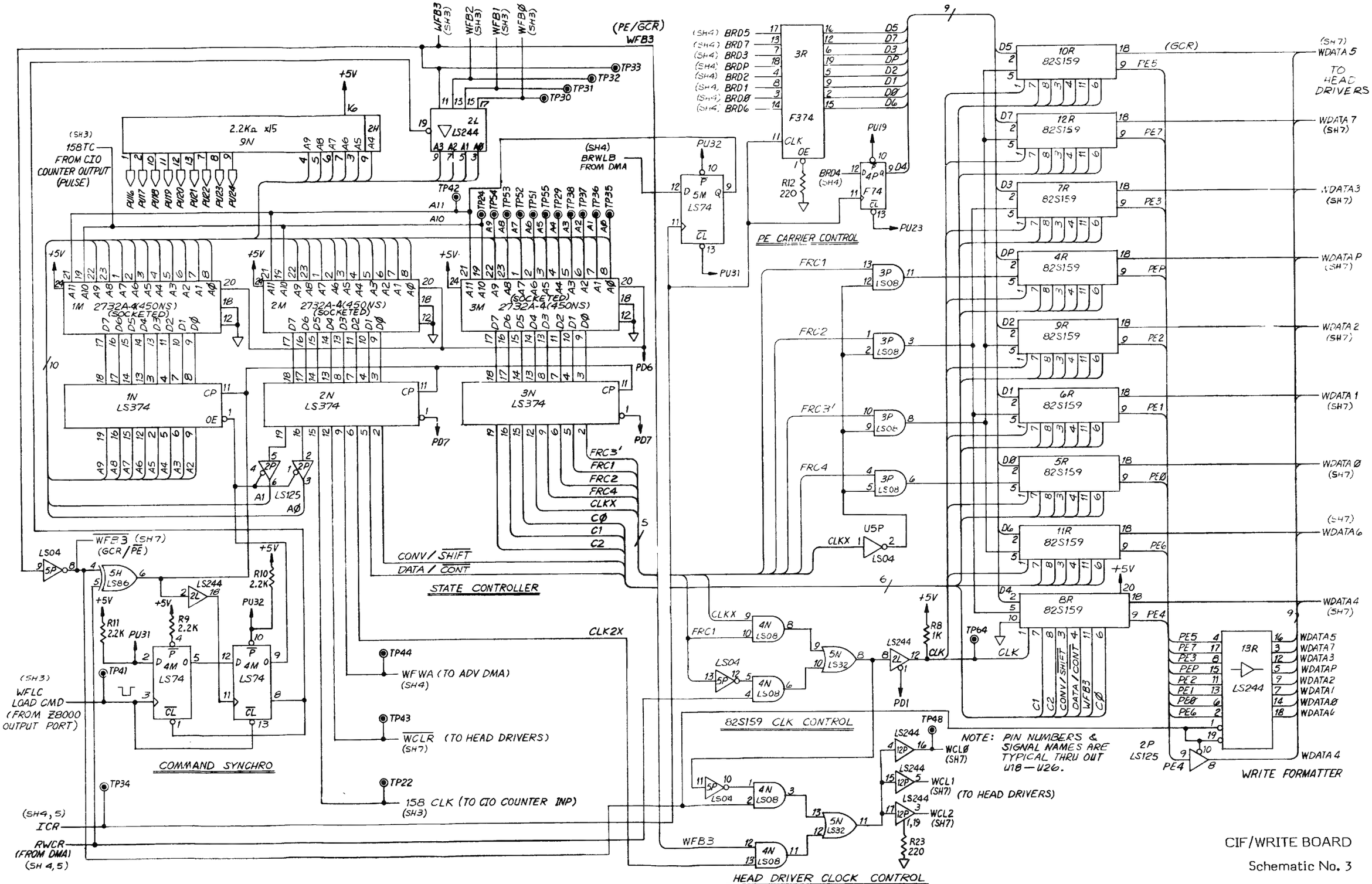
TEST MODE DATA REQUEST

DATA PATH PARITY ERROR

CIF CONTROL LOGIC

CIF/WRITE BOARD

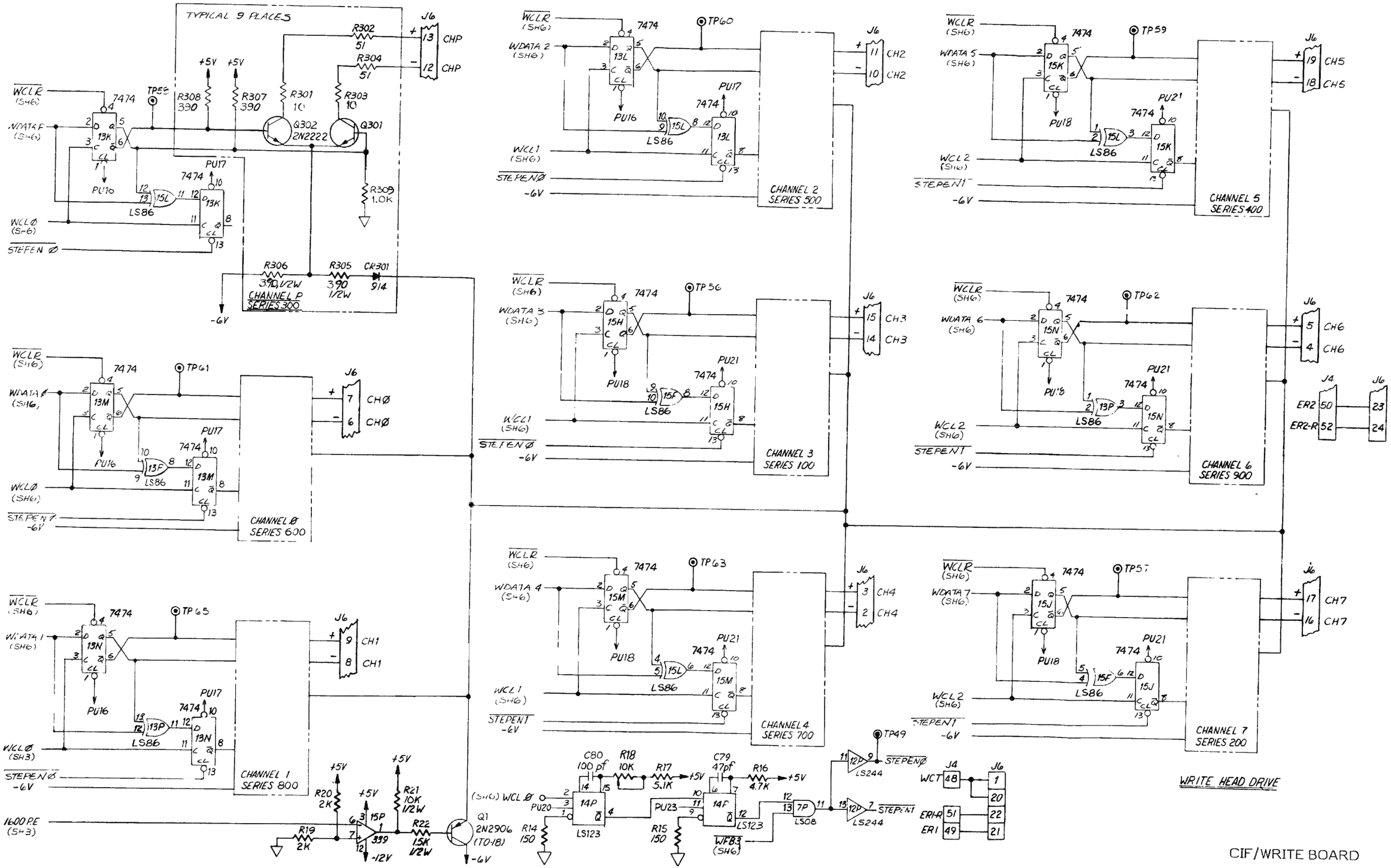
Schematic No. 3



CIF/WRITE BOARD

Schematic No. 3

Sht 6 of 7



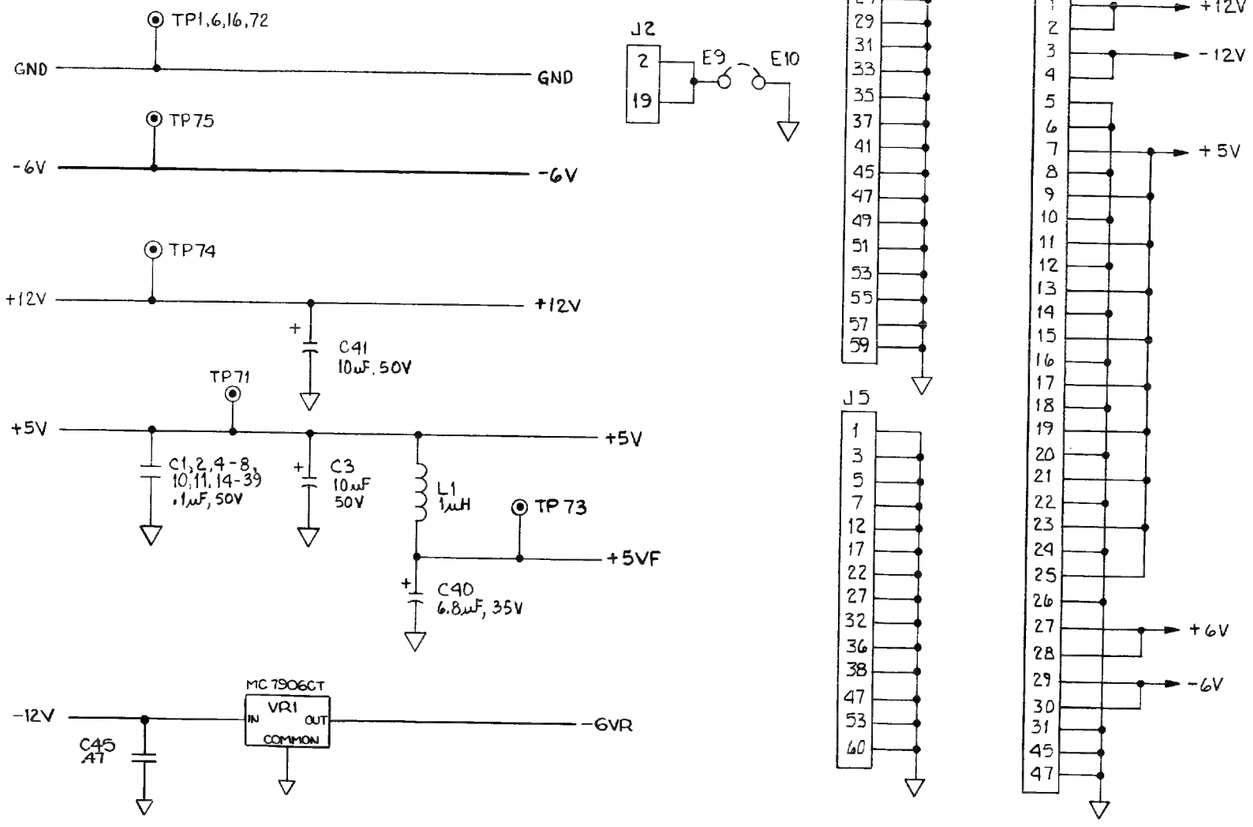
CIF/WRITE BOARD

Schematic No. 3

Sht 7 of 7

TYPE	REF DES	+12V	+5V	-6V	GND
C-5061	U15B, U15D, U15F, U15H, U15K, U15M, U15P, U15S U15U	6	10	1	5
'LS74	U10B, U11B, U12B, U11D, U12D, U10F, U11F, U12F, U11H, U12H, U10K, U11K, U12K, U11M, U12M, U10P, U11P, U12P, U11S, U12S, U10U, U11U, U12U, U4E		14		7
'S225	U9A, U10A, U9C, U10C, U9E, U10E, U9G, U10G, U9J, U10J, U9L, U10L, U9N, U10N, U9R, U10R, U9T, U10T		20		10
'LS273	U8A, U8C, U4C, U8E, U8G, U3H, U8J, U8N, U8R, U8T, U8L		20		10
'LS174	U6B, U6C, U10D, U1H, U2H, U4H U5H, U10H, U10M, U10S, U6J		16		8
2732A	U7A, U7C, U7E, U7F, U3G, U4G, U7J, U7L, U7N, U7R, U7T,		24		12
MC4044	U12A, U12T U12C, U12E, U12G, U12J, U12L, U12N, U12R		14		7
CD4066	U14A, U14C, U14E, U14J, U14L U14N, U14R, U14T, U14G		14	7	
'LS139	U8D, U8H, U8S, U8U, U8M		16		8
'LS00	U3B, U3J, U9B, U9F, U9K, U9P		14		7
'LS08	U4B, U2C, U3C, U2G, U8B, U8K, U8P		14		7
'LS244	U2A, U4A, U5A, U2B		20		10
'LS14	U1E		14		7
'LS245	U6A		20		10
'LS02	U6E		14		7
'LS04	U3E, U5E		14		7
'LS86	U1G		14		7
'LS198	U5G		16		8
'LS109	U2F, U9F		16		8
'LS125	U1F		14		7
'LS21	U1A		14		7
'LS32	U1C, U2E		14		7
24S41	U6G, U6H, U5J		18		9
8036	U5B		23		7
339	U5F		3		12
F79	U1B, U3F		14		7
6305-1	U6F		14		7
74221	U13B, U19B, U13D, U19D, U14F, U13F, U13H, U19H, U14K, U19M, U13P, U13K, U19P, U13S, U19S, U13U, U19U, U13M		16		8
79180	U3A		19		7

REFERENCE DESIGNATIONS			
LAST USED	NOT USED	LAST USED	NOT USED
R60			
C45			
L1			
Q2			
TP75			
VR1			

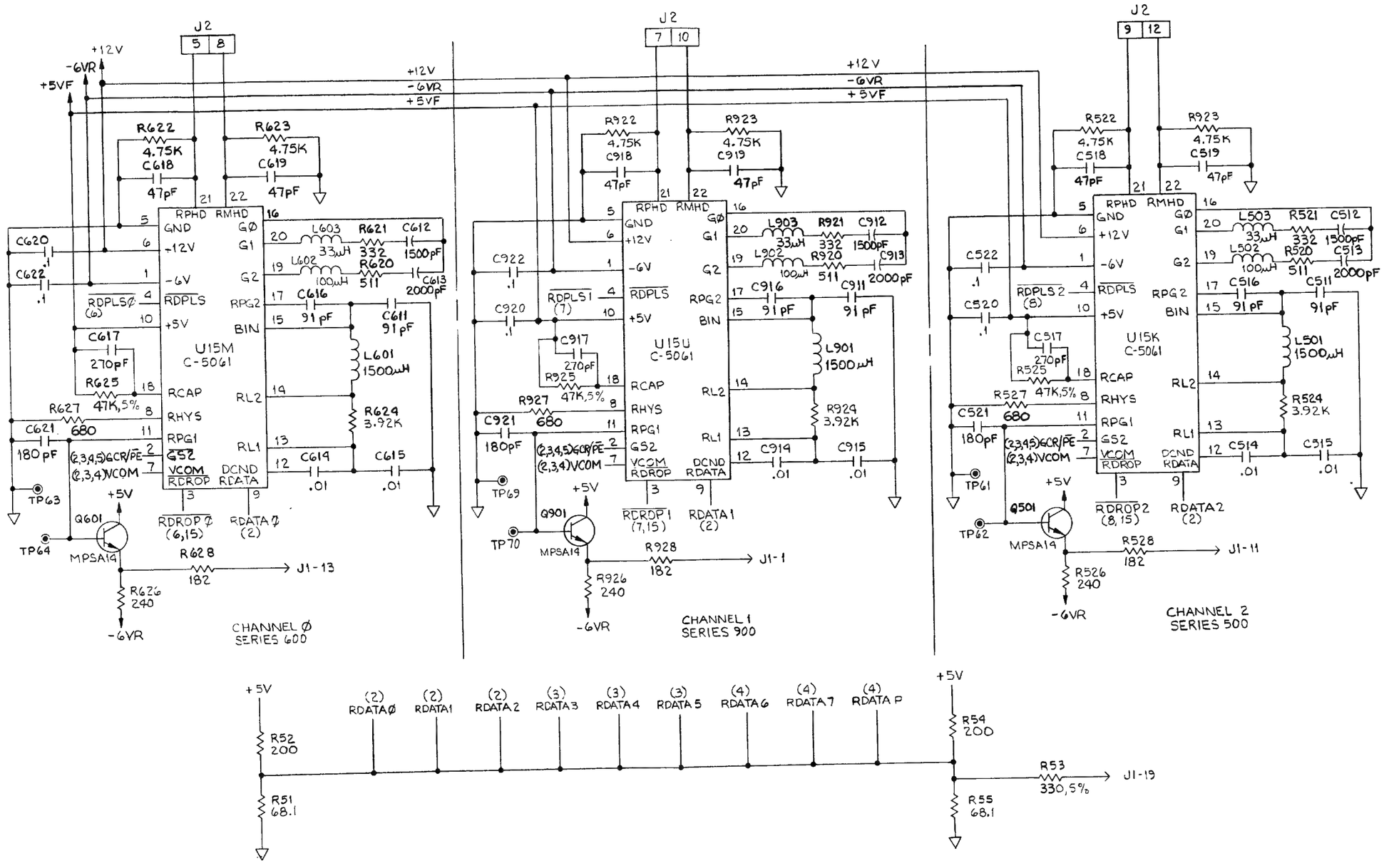


4. ALL RESISTORS 1% TO BE 1/8W, ALL 5% TO BE 1/4W
3. X= SERIES NO.(100-900) IN WHICH THE COMPONENTS APPEARS
2. ALL INDUCTORS ARE IN MICROHENRYS
1. ALL CAPACITORS ARE IN MICROFARADS

NOTES: UNLESS OTHERWISE SPECIFIED

DATA BOARD

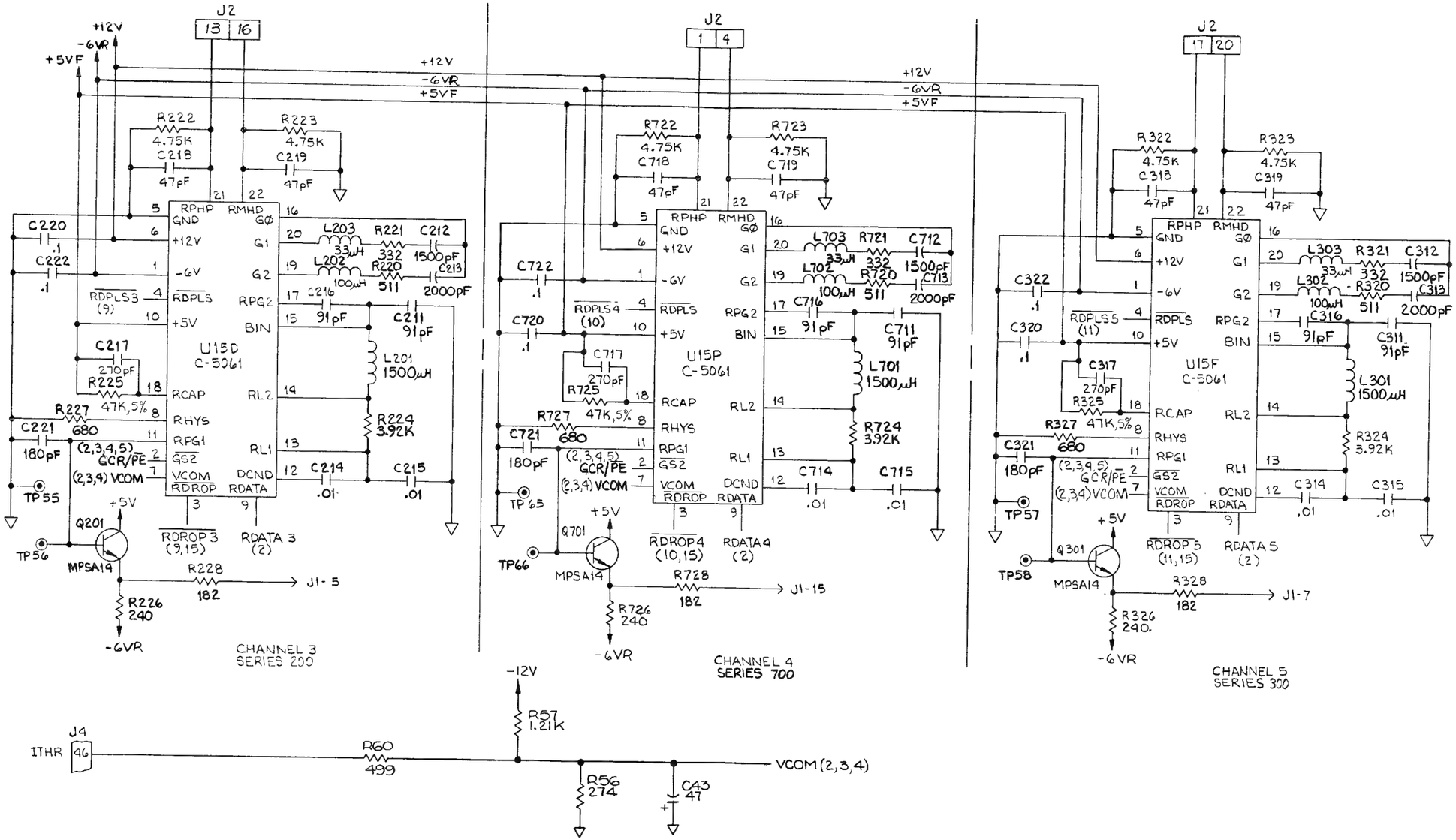
Schematic No. 4



DATA BOARD

Schematic No. 4

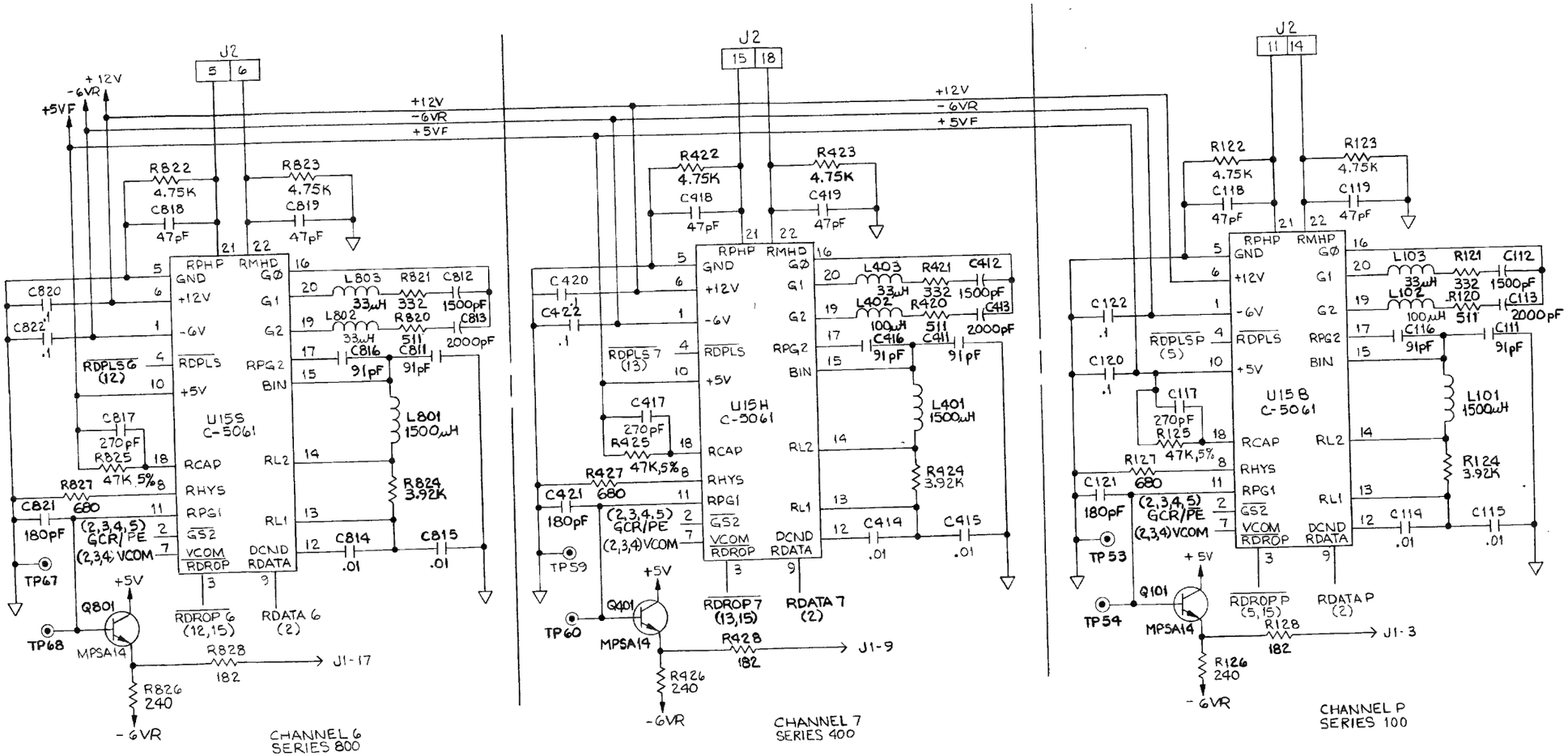
Sht 2 of 15



DATA BOARD

Schematic No. 4

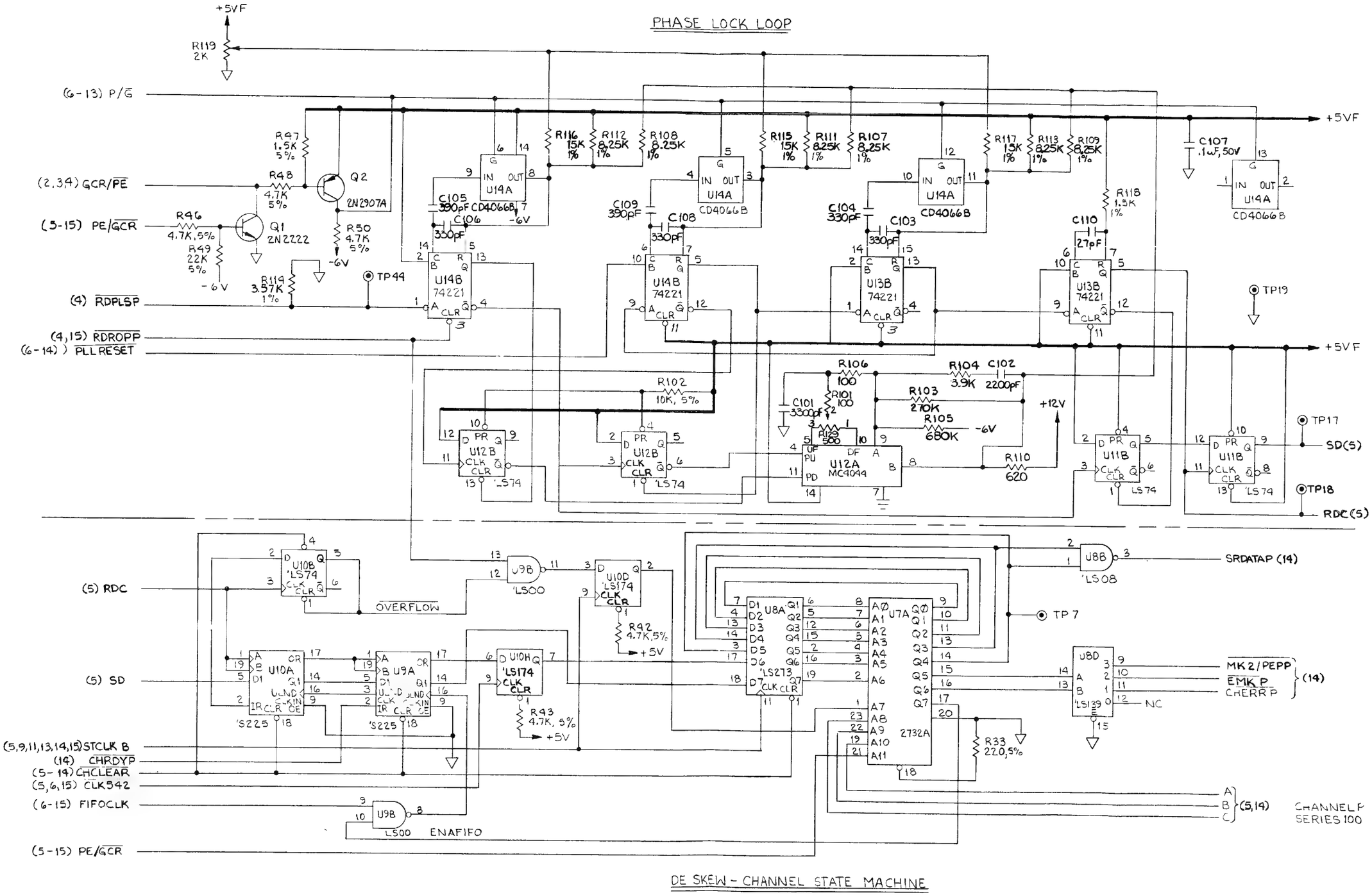
Sht 3 of 15



DATA BOARD

Schematic No. 4

PHASE LOCK LOOP



DE SKEW - CHANNEL STATE MACHINE

DATA BOARD

Schematic No. 4

PHASE LOCK LOOP

+5VF
R619 2K
(5,7-13)P/G
+5VF
R616 15K 1%
R612 8.25K 1%
R608 8.25 1%
R615 15K 1%
R611 8.25K 1%
R607 8.25K 1%
R617 15K 1%
R613 8.25K 1%
R609 8.25K 1%
C607 .1 uF, 50V
U14L CD4066B
C605 390pF
C606 330pF
-6V
C609 390pF
C608 330pF
C604 390pF
C603 330pF
R618 1.5K 1%
C610 27pF
R614 3.57K 1%
TP49
TP34
(2) RDPLS Ø
U14M 74221
U13M 74221
(2,15) RDROP Ø
(5,7-19) PLL RESET
+5VF
R602 10K, 5%
R606 100
R604 3.9K
C602 2200pF
C601 3300pF
R601 100
R603 270K
R605 680K
-6V
+12V
U12M 'LS74
U12L MC4044
R610 620
U11M 'LS74
TP32
SD (6)
TP33
RDC (6)

(6) RDC
U10K 'LS74
OVERFLOW
U9K 'LS00
U10M 'LS174
R44 4.7K, 5% +5V
U8K 'LS08
SR DATA Ø (19)
TP12
U8L 'LS273
U7L 2732A
U8M 'LS139
MK2/PEP Ø
EMK Ø
CHERR Ø
(19)
NC
(6) SD
U10L OR 'S225
U9L OR 'S225
U10S 'LS174
R45 4.7K, 5% +5V
R38 220, 5%
(7,8,10,12,15) STCLK A
(14) CHRDY Ø
(5,7-14) CHCLEAR
(5,6,15) CLK 542
(5,7-15) FIFOCLK
U9K 'LS00 ENAFIFO
(5,7-15) DE/SCR
A
B
C
(5,7-14) CHANNEL Ø SERIES 600

DE SKEW - CHANNEL STATE MACHINE

DATA BOARD
Schematic No. 4
Sht 6 of 15

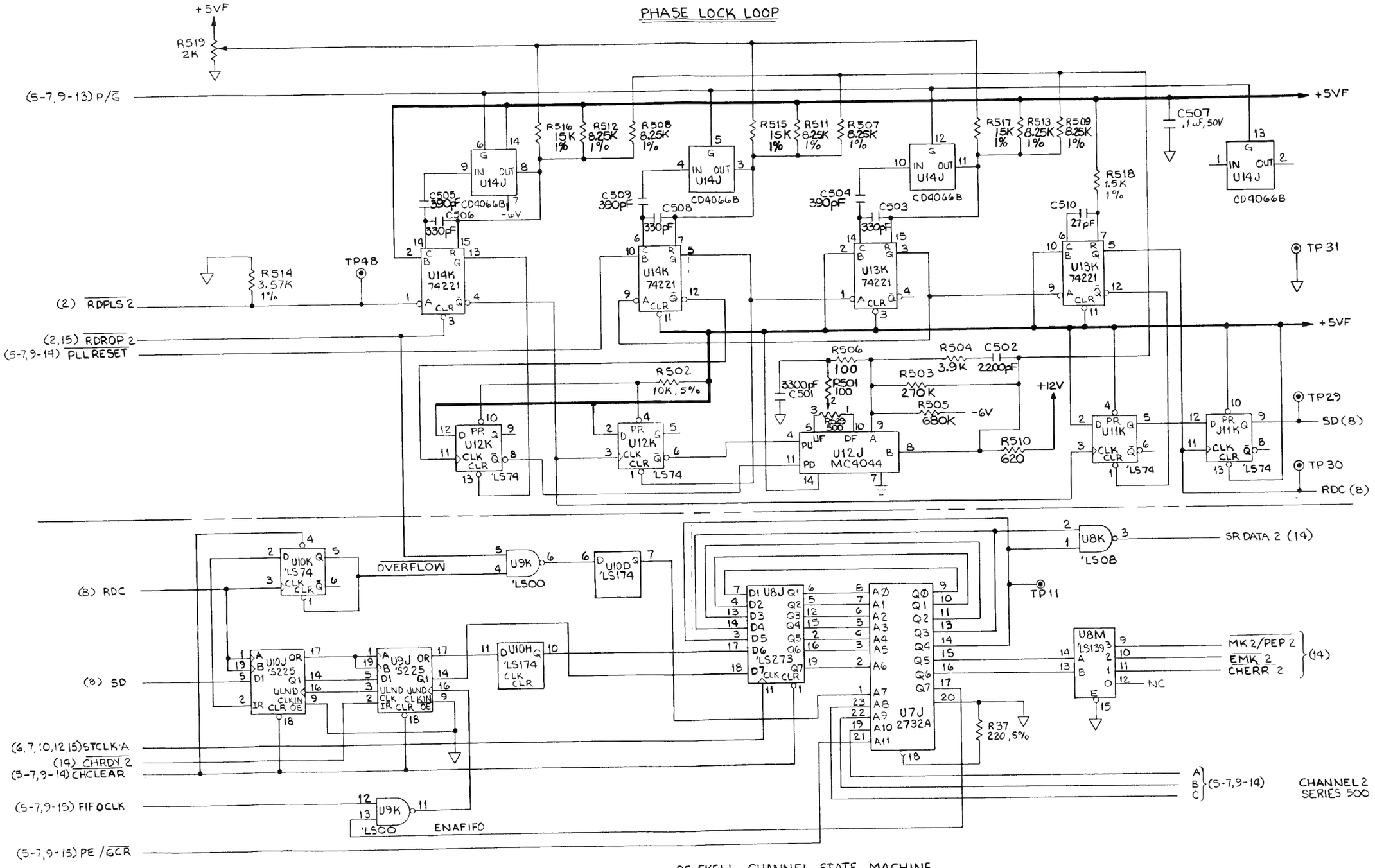
PHASE LOCK LOOP

+5VF
R919 2K
(5,6,8-13) P/$\overline{G}$
+5VF
R916 15K 1%
R912 8.25K 1%
R908 8.25K 1%
R915 15K 1%
R911 8.25K 1%
R907 8.25K 1%
R917 15K 1%
R913 8.25K 1%
R909 8.25K 1%
C907 .1uF,50V
R918 1.5K 1%
U14T CD4066B
C905 330pF
C906 330pF
C909 390pF
C908 330pF
C904 390pF
C903 330pF
C910 27pF
-6V
R914 3.57K 1%
TP52
(2) $\overline{RDPLS1}$
(2,15) $\overline{RDROP1}$
(5,6,8-19) $\overline{PLLRESET}$
U14U 74221
U13U 74221
TP43
+5VF
R902 10K, 5%
R906 100
R904 3.9K
C902 2200pF
C901 3300pF
R901 100
R903 270K
R905 680K
6V
+12V
R910 620
R929 500
U12T MC4044
U12U 'LS74
U11U 'LS74
TP41
SD (7)
TP42
RDC (7)

(7) RDC
(7) SD
(6,8,10,12,15) STCLK A
(14) $\overline{CHRDY1}$
(5,6,8-19) $\overline{CHCLEAR}$
(5,6,8-15) FIFOCLK
(5,6,8-15) PE/$\overline{GCR}$
U10U 'LS74
U10T 'S225
U9T 'S225
U9U 'LS00
U10S 'LS174
U10M 'LS174
OVERFLOW
ENAFIFO
U8T 'LS273
U7T 2732A
U8P 'LS08
SR DATA 1 (14)
TP15
U8U 'LS139
MK2/PEP1
$\overline{EMK1}$
$\overline{CHERR1}$
(14)
NC
R41 220, 5%
A
B
C
(5,6,8-19)
CHANNEL1
SERIES 900

DE SKEW - CHANNEL STATE MACHINE

DATA BOARD
Schematic No. 4

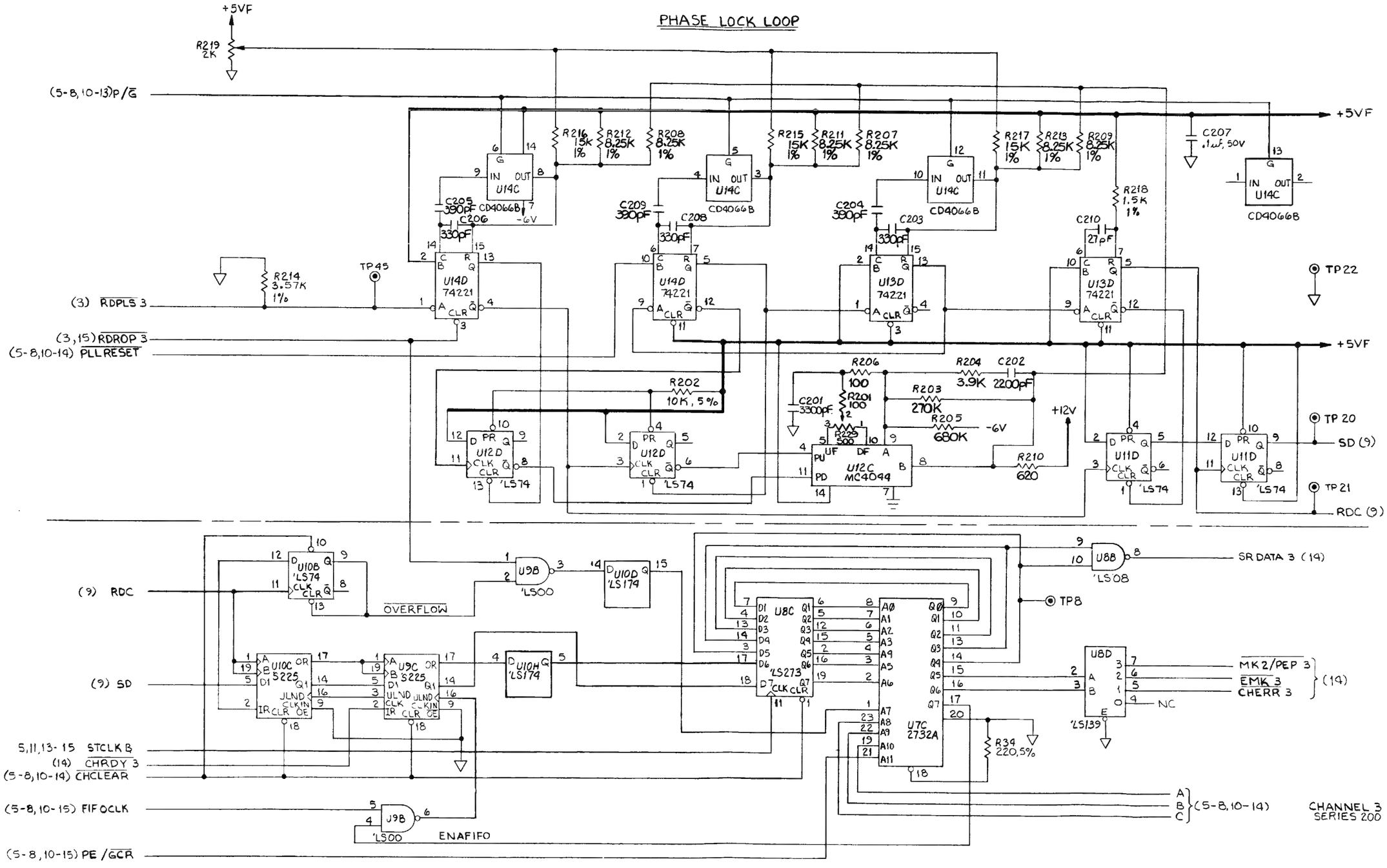


DE SKEW - CHANNEL STATE MACHINE

DATA BOARD

Schematic No. 4

PHASE LOCK LOOP



DE SKEW - CHANNEL STATE MACHINE

DATA BOARD

Schematic No. 4

PHASE LOCK LOOP

+5VF
R719 2K
(5-9,11-13)P/G
+5VF
R716 15K 1%
R712 8.25K 1%
R708 8.25K 1%
R715 15K 1%
R711 8.25K 1%
R707 8.25K 1%
R717 15K 1%
R713 8.25K 1%
R709 8.25K 1%
C707 .1 uF, 50V
R718 1.5K 1%
U14N CD4066B
C705 390pF
C706 330pF
C709 390pF
C708 330pF
C704 390pF
C703 330pF
C710 27 pF
-6V
R714 3.57K 1%
TP50
(3) RDPLS4
(3-15) RDROP4
(5-9,11-14) PLL RESET
U14P 74221
U13P 74221
TP37
+5VF
R702 10K, 5%
R706 100
R704 3.9K
C702 2200pF
R703 270K
R701 100
C701 3300pF
R705 680K
-6V
+12V
R710 620
U12N MC4044
U12P 'LS74
U11P 'LS74
TP35
SD (10)
TP36
RDC (10)

(10) RDC
(10) SD
OVERFLOW
U10P 'LS74
U9P 'LS00
U10M 'LS174
U10N OR S225
U9N OR S225
U10S 'LS174
U8N 'LS273
U7N 2732A
U8P 'LS08
SR DATA 4 (19)
TP13
U8S 'LS139
MK2/PEP 4
EMK 4
CHERR 4
(14)
NC
R39 220, 5%
(6,7,8,12,15) STCLK A
(14) CHRDY 4
(5-9,11-14) CHCLEAR
(5-9,11-15) FIFOCLK
ENAFIFO
(5-9,11-15) PE /GCR
A
B
C
(5-9,11-14)
CHANNEL 4
SERIES 700

DE SKEW - CHANNEL STATE MACHINE

DATA BOARD
Schematic No. 4

PHASE LOCK LOOP

+5VF
R319 2K
(5-10,12-13) P/$\overline{G}$
R316 15K 1%
R312 8.25K 1%
R308 8.25K 1%
R315 15K 1%
R311 8.25K 1%
R307 8.25K 1%
R317 15K 1%
R313 8.25K 1%
R309 8.25K 1%
C307 .1uF, 50V
R318 1.5K 1%
C305 390pF
C306 330pF
C309 390pF
C308 330pF
C304 390pF
C303 330pF
C310 27pF
U14E CD4066B
-6V
R314 3.57K, 1%
TP46
(3) $\overline{RDPLS}$ 5
(3,15) $\overline{RDROPS}$
(5-10,12-14) PLL RESET
U14F 74221
U13F 74221
TP25
R302 10K, 5%
R306 100
R301 100
C301 3300pF
R329 500
R303 270K
R305 680K
R304 3.9K
C302 2200pF
+12V
R310 620
U12F 'LS74
U12E MC9044
U11F 'LS74
TP23
SD (11)
TP24
RDC (11)

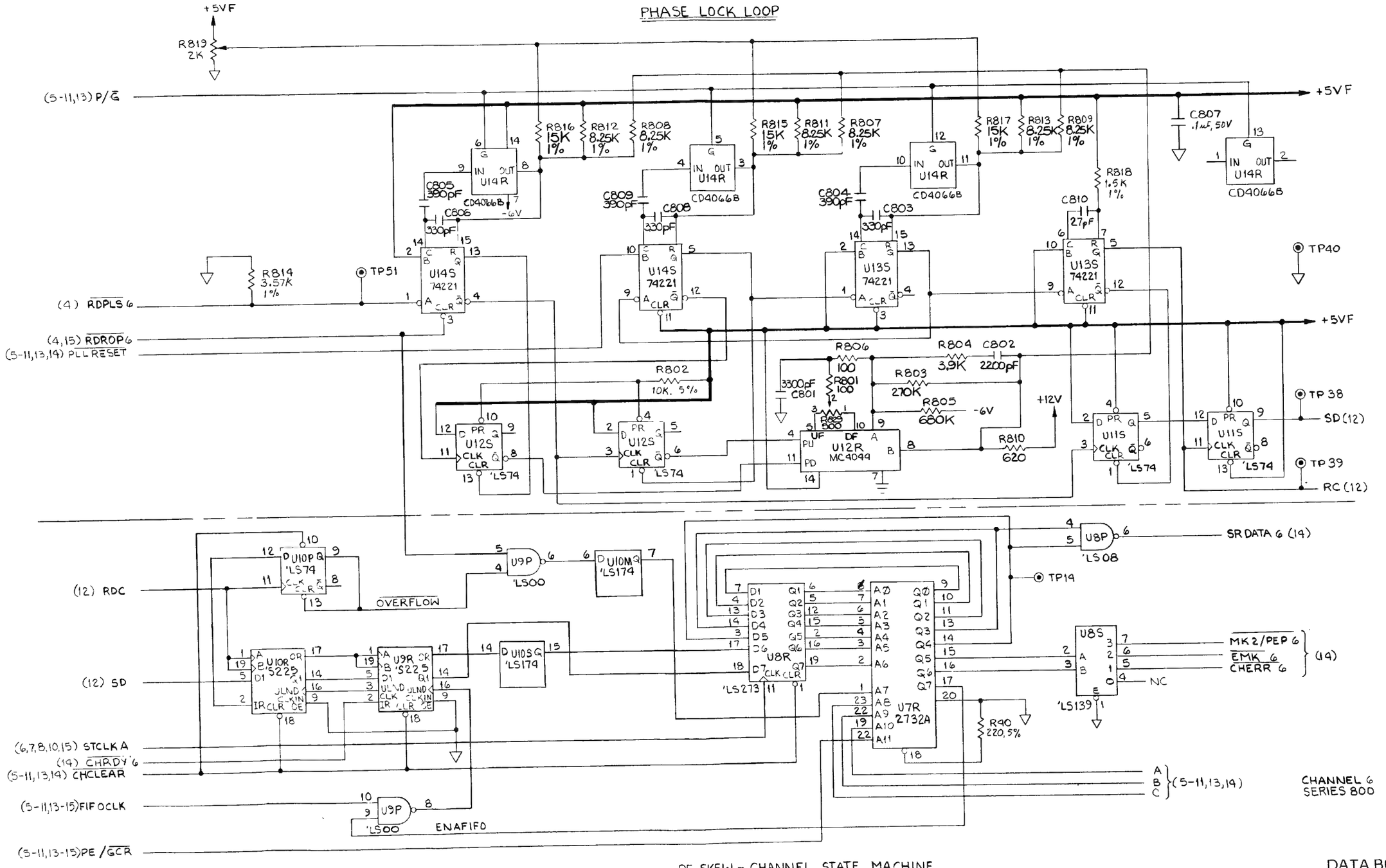
(11) RDC
(11) SD
(5,9,13-15) STCLK B
(14) $\overline{CHRDY}$ 5
(5-10,12-14) $\overline{CHCLEAR}$
(5-10,12-15) FIFOCLK
(5-10,12-15) PE /$\overline{GCR}$
U10F 'LS74
U9F 'LS00
U10D 'LS174
OVERFLOW
U10E 'S225
U9E 'S225
U10H 'LS174
ENAFIFO
U8E 'LS273
U7E 2732A
R35 220, 5%
U8K 'LS08
SR DATA 5 (14)
TP9
U8H 'LS139
MK2/PEP 5
$\overline{EMK}$ 5
CHERR 5
(14)
NC
A
B
C
(5-10,12-14)

CHANNEL 5
SERIES 300

DE SKEW - CHANNEL STATE MACHINE

DATA BOARD
Schematic No. 4

PHASE LOCK LOOP



DE SKEW - CHANNEL STATE MACHINE

CHANNEL 6
SERIES 800

DATA BOARD

Schematic No. 4

PHASE LOCK LOOP

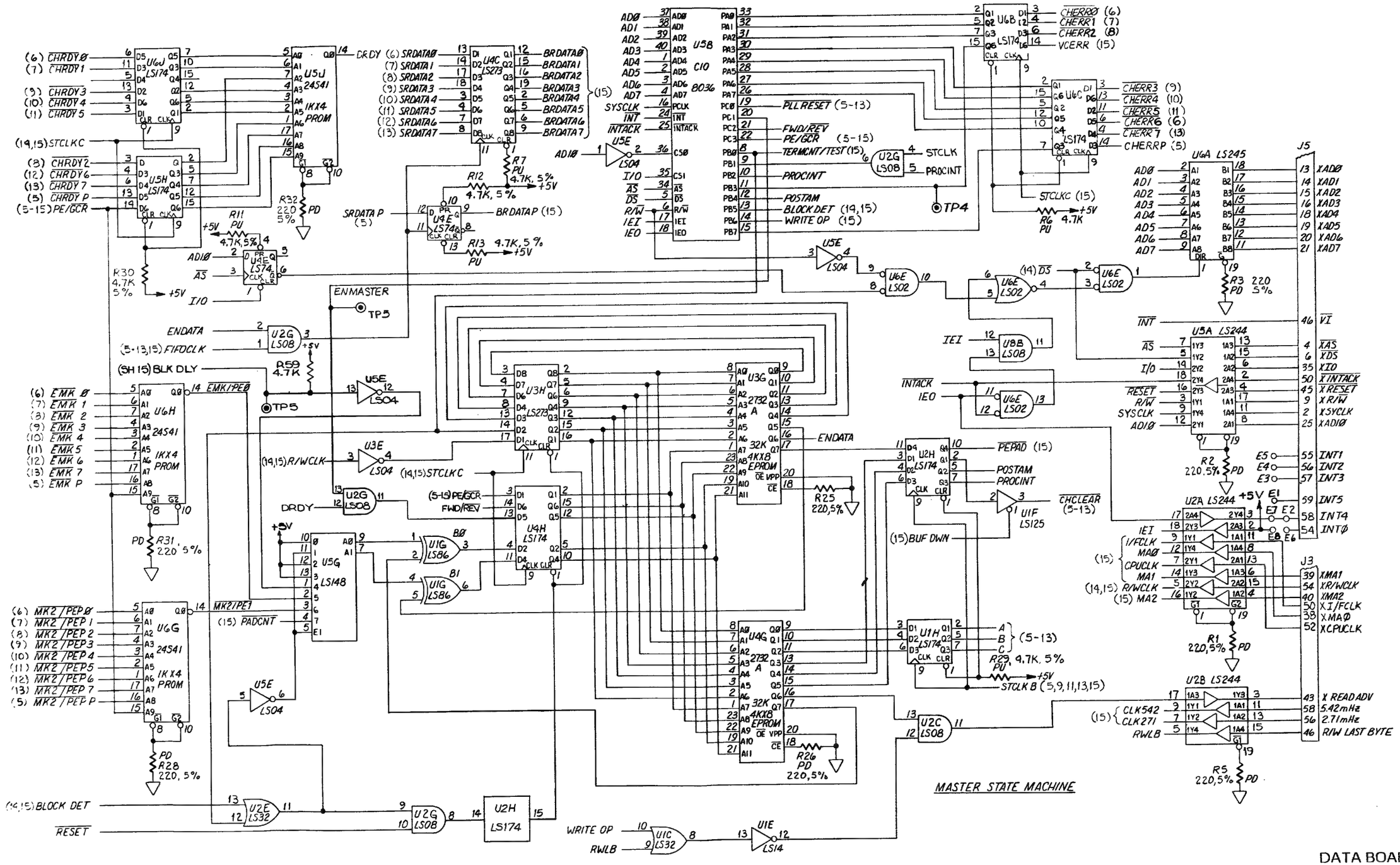
+5VF
R419 2K
(5-12) P/$\overline{G}$
R416 15K 1%
R412 8.25K 1%
R408 8.25K 1%
R415 15K 1%
R411 8.25K 1%
R407 8.25K 1%
R417 15K 1%
R413 8.25K 1%
R409 8.25K 1%
C407 .1 uF, 50V
R418 1.5K 1%
C410 27pF
C405 390pF
C406 330pF
C409 390pF
C408 330pF
C404 390pF
C403 330pF
U14G CD4066B
-6V
R414 3.57K 1%
TP47
(4) RDPLS 7
(4,15) RDROP 7
(5-12,14) PLLRESET
U14H 74221
U13H 74221
TP28
R402 10K, 5%
R406 100
R403 270K
R404 3.9K
C402 2200pF
C401 3300pF
R401 100
R405 680K
R410 620
+12V
U12H 'LS74
U12G MC4044
U11H 'LS74
TP26
SD (13)
TP27
RDC (13)

(13) RDC
U10F LS74
OVERFLOW
U9F LS00
U8K LS08
SR DATA 7 (14)
TP10
(14) $\overline{CHRDY}$ 7
(13) SD
U10G OR S225
U9G OR S225
U10H LS174
U10M LS174
U8G LS273
U7F 2732A
U8H 'LS139
$\overline{MK2/PEP}$ 7
$\overline{EMK}$ 7
$\overline{CHERR}$ 7
(14)
NC
R36 220, 5%
(5-12,14) $\overline{CHCLEAR}$
(5-12,14,15) FIFOCLK
U9F LS00
ENAFIFO
(5-12 14,15) PE/$\overline{GCR}$
(5,9,11,14,15) STCLK B
A
B
C
(5-12,14)

CHANNEL 7
SERIES 400

DE SKEW - CHANNEL STATE MACHINE

DATA BOARD
Schematic No. 4



DATA BOARD

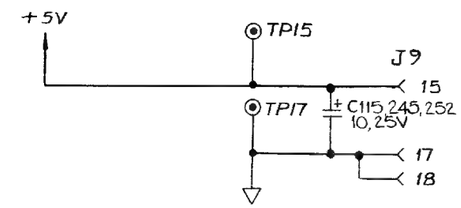
Schematic No. 4

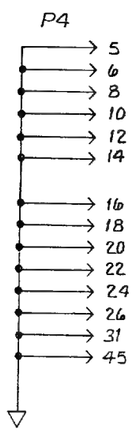
(14,15) CLK542
(14) CLK271
(14,15) R/W CLK
(14,15) CPU CLK
(5-14) FIFOCLK
U5E LS04
U3E LS04
U2C LS08
U2E LS32
PU R19 4.7K,5%
+5V
U3F F74
R18 PU 4.7K,5%
U2C LS08
U2F LS109
PU R17 4.7K,5%
CLOCK GENERATION LOGIC
U1E LS14
R8 330,5%
C9 47pF
TP 2
U1F LS125
STCLKA (6,7,8,10,12)
STCLKB (5,9,11,13,14)
STCLKC (14) (19)
+5V
PU R10 4.7K,5%
U3E LS04
BUF DWN (19)
CLK542 (5,6)
PE/GCR (5-15)
MA0
MA1
MA2
(14)
PU R4 4.7K,5%
U1A LS21
U1B F74
WRITE OP
U2E LS32
PADCNT (14)
U2C LS08
(19,15) CPUCLK
U3E LS04
U1C LS32
I/F CLK
TERMCNT/TEST
(14)
PEPAD
BR DATA Ø
BR DATA 1
BR DATA 2
BR DATA 3
BR DATA 4
BR DATA 5
BR DATA 6
BR DATA 7
BR DATA P
(14)
U3C LS08
U3 LS08
U4B LS08
U4A LS244
U2B LS244
U3E LS04
R/WCLK (14,15)
U4B LS08
U4F LS109
U3B LS00
U3A 180
EVEN
ODD
VRCERR (14)
U1E LS14
J3
MWDØ
MWD1
MWD2
MWD3
MWD4
MWD5
MWD6
MWD7
MWDP
+5V
R22 200K 1%
R20 200K 1%
R14 3.92K 1%
R15 10K 5%
R16 10K 5%
U5F LM339
U4F LS109
(4,5) RDROP P
(2,6) RDROP Ø
(2,7) RDROP 1
(2,8) RDROP 2
(3,9) RDROP 3
(3,10) RDROP 4
(3,11) RDROP 5
(9,12) RDROP 6
(9,13) RDROP 7
U6F-1 6305 PROM
C12 470pF
R24 162K 1%
R27 220,5%
R23 162K 1%
C13 470pF
R21 1.0K 1%
U5F LM339
U5E LS09
(5-15) PE/GCR
(14,15) CLK542
(19) BLOCK DET
BLOCK DETECTION
R58 200K Ω 1/8W 1%
C44 470 PF
U5F LM339
BLK DLY (SH14)

DATA BOARD
Schematic No. 4

REFERENCE DESIGNATION		
LTR	LAST USED	NOT USED
C	283	
CR	86	
DS	1	
J	9	2,3,4,5
K	1	
L	11	
Q	46	
R	353	
T	2	
U	17V	
VR	6	
TP	37	

IC TYPE	REFERENCE DESIGNATOR	+5V	GND	+12	-12	+6	-6
74LS08	U17S, 14E, 14F	14	7				
74LS11	U17P, 17T	14	7				
74LS14	U15E	14	7				
74LS04	U13H	14	7				
74LS74	U15R	14	7				
74LS123	U16M, 17R	16	8				
74LS138	U12E	16	8				
74LS175	U11E, 12C	16	8				
74LS378	U13A, 13C	16	8				
74LS244	U11C	20	10				
74LS00	U12H	14	7				
74LS32	U12F	14	7				
7406	U7C	14	7				
7407	U9H 17V	14	7				
7414	U7E, 16N	14	7				
TL082	U8A 8B, 11A, 11B			8	4		
LM339	U3E, 7G, 12K, 16H, 15P, 15T, 8W, 15N			3	12		
LM3525A	U5G		12				
NE556N	U5E	14	7				
RC4136	U16K, 16L, 15S, 15V, 6W			11	7		
MD14051	U10A, 10E		8			16	7
AD7533LN	U12A	15	3	14	3		
ADC1001	U13E	20	10				
Z8036	U14A, 16A	23	7				





SENSE/SERVO BOARD

Schematic No. 5

Sht 1 of 7

SENSE/SERVO BOARD

Schematic No. 5

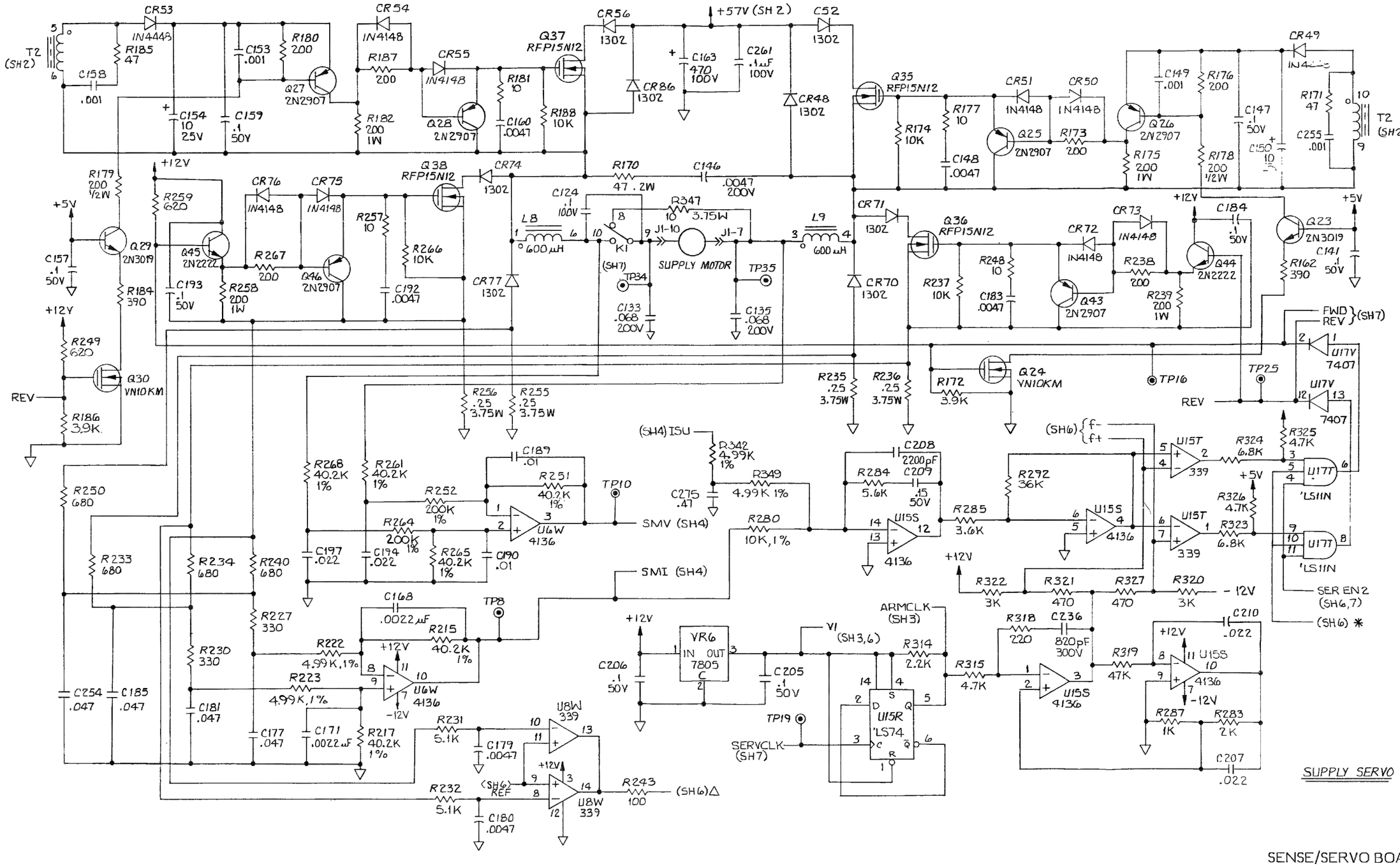
ERASE HEAD DRIVER

WRITE CENTER TAP HEAD DRIVER

SENSE/SERVO BOARD
Schematic No. 5

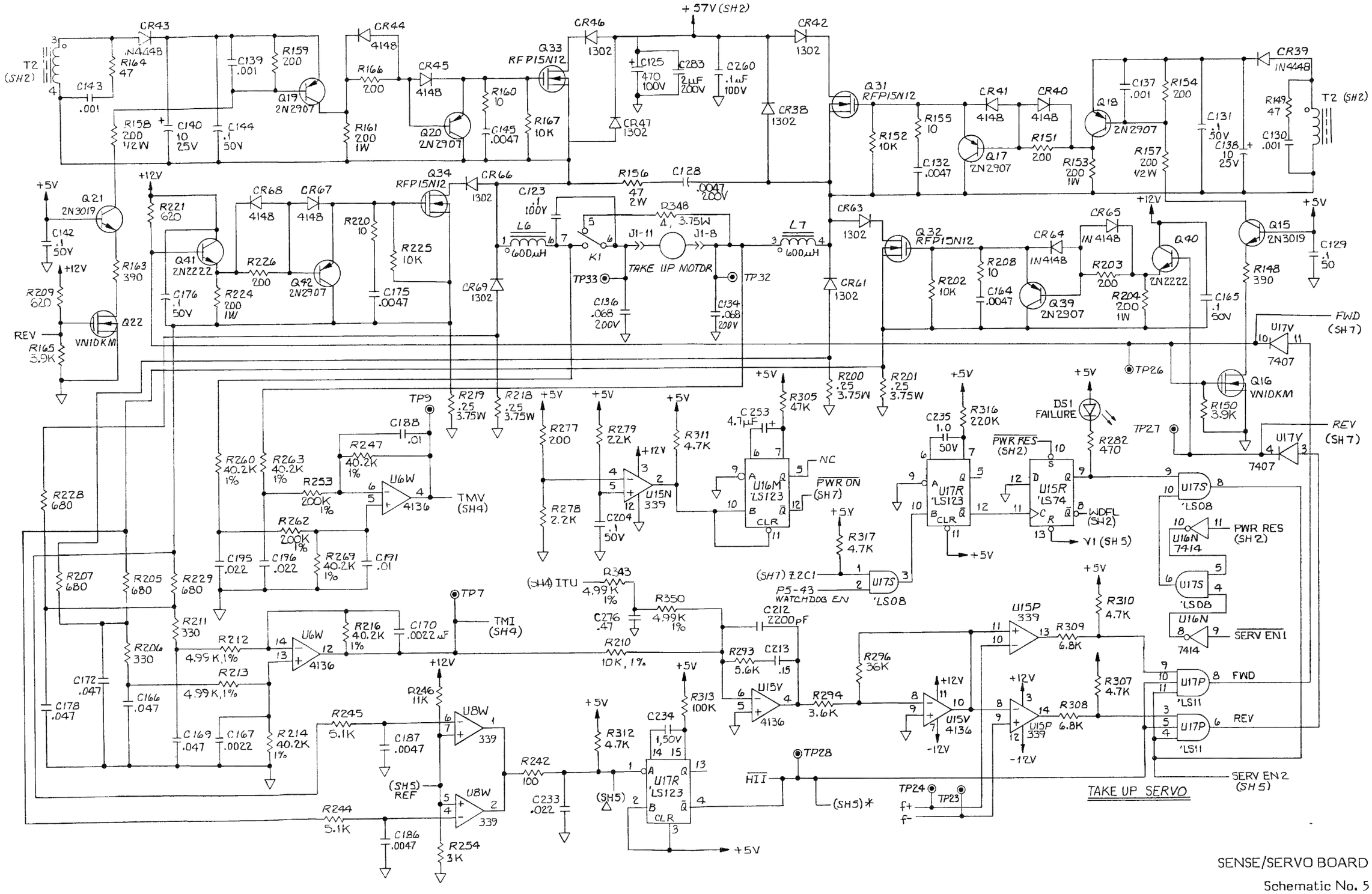
SENSE/SERVO BOARD

Schematic No. 5



SENSE/SERVO BOARD

Schematic No. 5



SENSE/SERVO BOARD

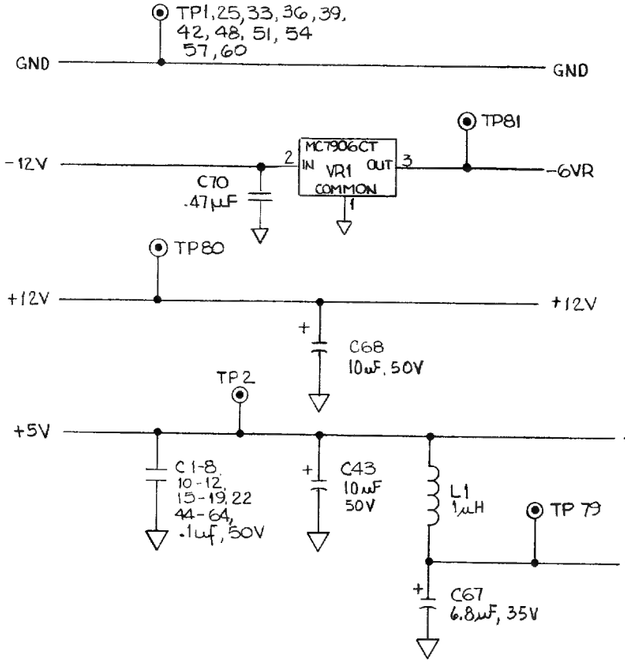
Schematic No. 5

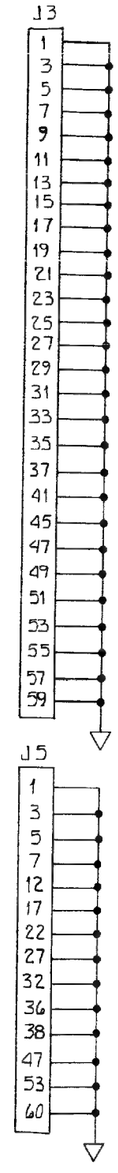
SENSE/SERVO BOARD

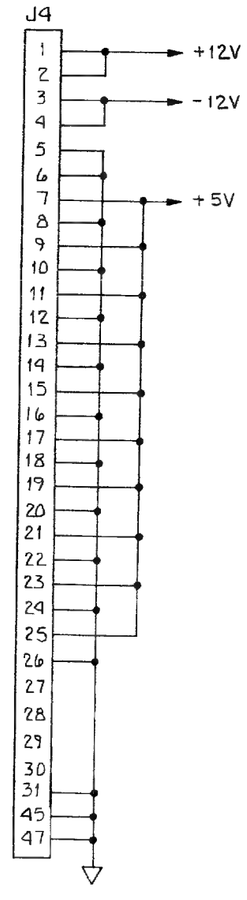
Schematic No. 5

TYPE	REF DES	+12V	+5V	-6V	GND
C-5061	U26B, U26D, U26F, U26H, U26K, U26M, U26P, U26S, U26U	6	10	1	5
'LS74	U21B, U22B, U23B, U22D, U23D, U22S, U20G, U22F, U23F, U22H U23H, U21J, U22K, U23K, U22M, U23M, U21P, U22P, U23P, U21U, U23U, U10E, U23S, U22U		14		7
'S225	U20A, U21A, U20C, U21C, U20E, U21E, U20F, U21F, U20H, U21H, U21N, U20L, U20N, U21L, U20R, U21R, U20T, U21T		20		10
'LS273	U19A, U19C, U10C, U19E, U19F, U19L, U19R, U6H, U19H, U19N, U19T		20		10
'LS174	U15B, U15C, U21D, U1H, U3H, U10H U12H, U21G, U21M, U21S, U15J		16		8
2732A	U18A, U18C, U18E, U18F. U18J, U18L, U18N, U18R, U18T, U5G, U10G		24		12
MC4044	U23A, U23C, U23E, U23G, U23J, U23L, U23N, U23R, U23T		14		7
CD4066	U25A, U25C, U25E, U25G, U25J, U25L, U25N, U25R, U25T		14		7
'LS139	U19D, U19G, U19S, U19M, U18U		16		8
'LS00	U20B, U20D, U20J, U20P, U20U, U6B		14		7
'LS08	U3C, U3G, U6C. U10B, U19B, U19J, U19P,		14		7
LS244	U10A, U12A, U3A, U3B		20		10
'LS14	U1E		14		7
'LS245	U15A		20		10
'LS02	U15E		14		7
'LS04	U6E, U12E		14		7
'LS86	U1G		14		7
'LS198	U12G		16		8
'LS109	U3F, U10F		16		8
'LS125	U1F		14		7
'LS21	U1A		14		7
'LS32	U1C, U3E		14		7
29S41	U12J, U15H, U15G		18		9
8036	U12B		23		7
339	U12F		3		12
F79	U1B, U6F		14		7
6305-1	U15F		14		7
74221	U24B, U24D, U25D, U25F U25B, U25K, U24F, U24H, U25H, U25M, U24P, U25P, U24S, U25S, U24U, U25U, U24K, U24M		16		8
74180	U6A		14		7

REFERENCE DESIGNATIONS			
LAST USED	NOT USED	LAST USED	NOT USED
R			
C			
L			
Q			
TP			

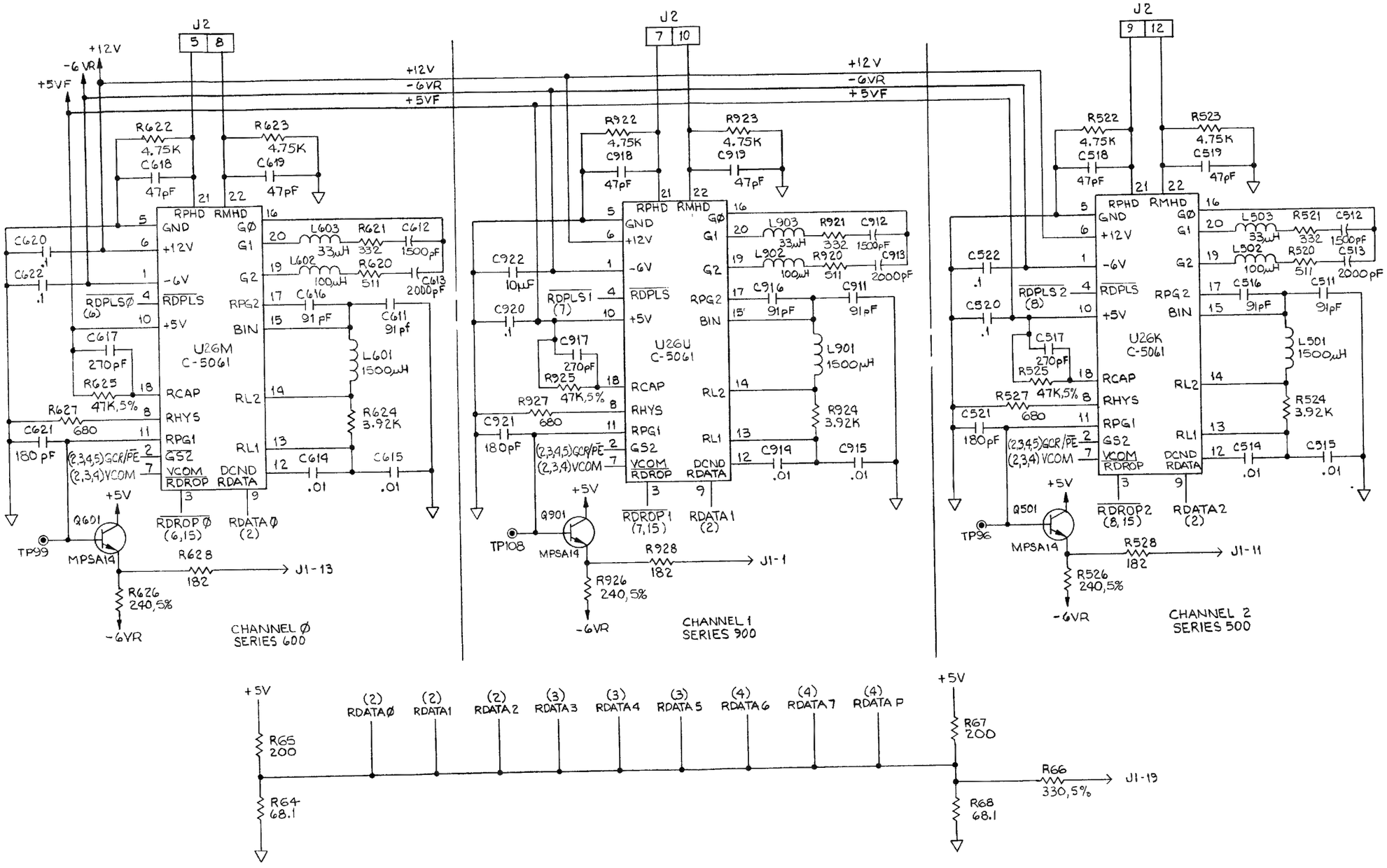






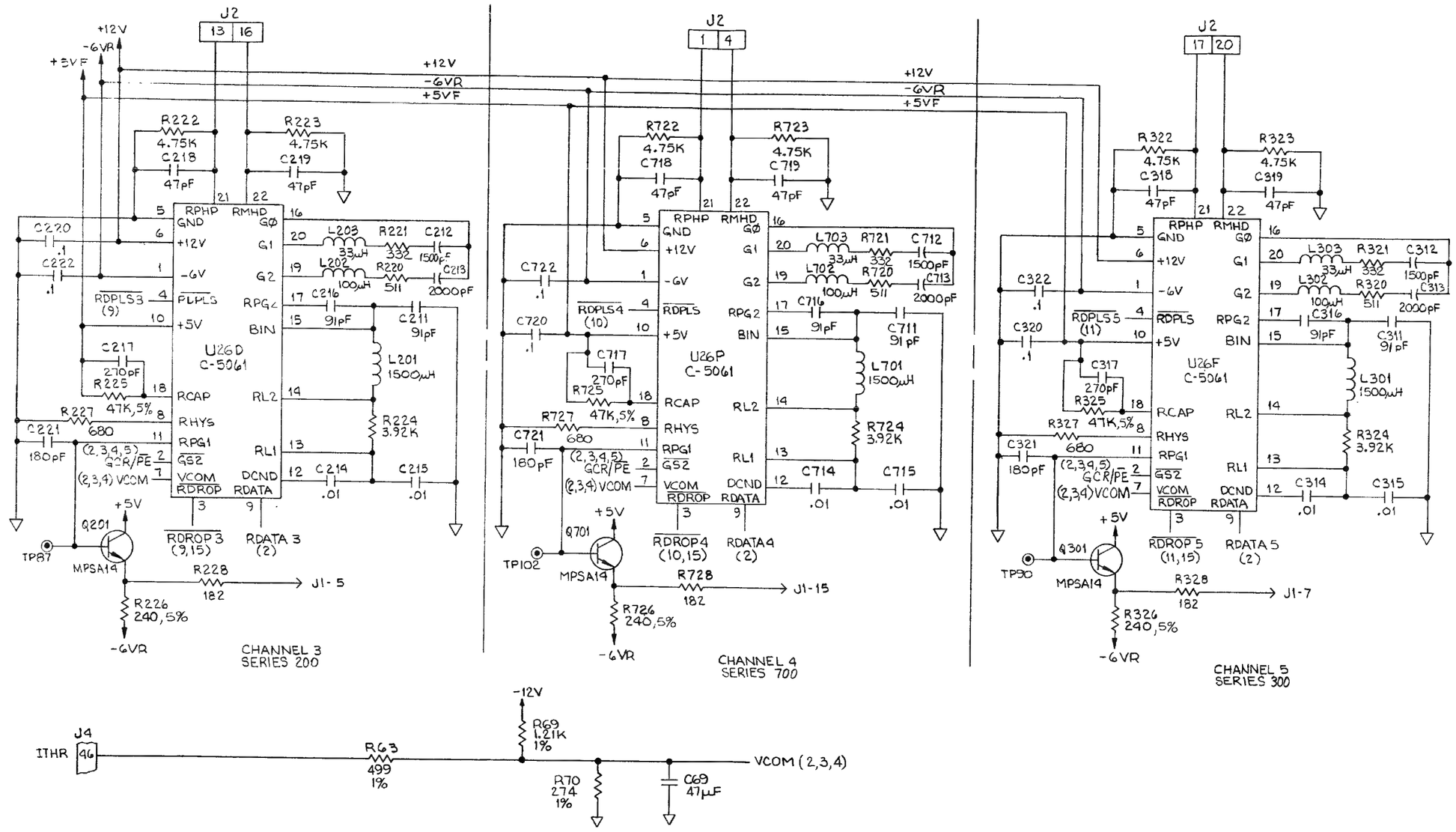
DATA BOARD

Schematic No. 6



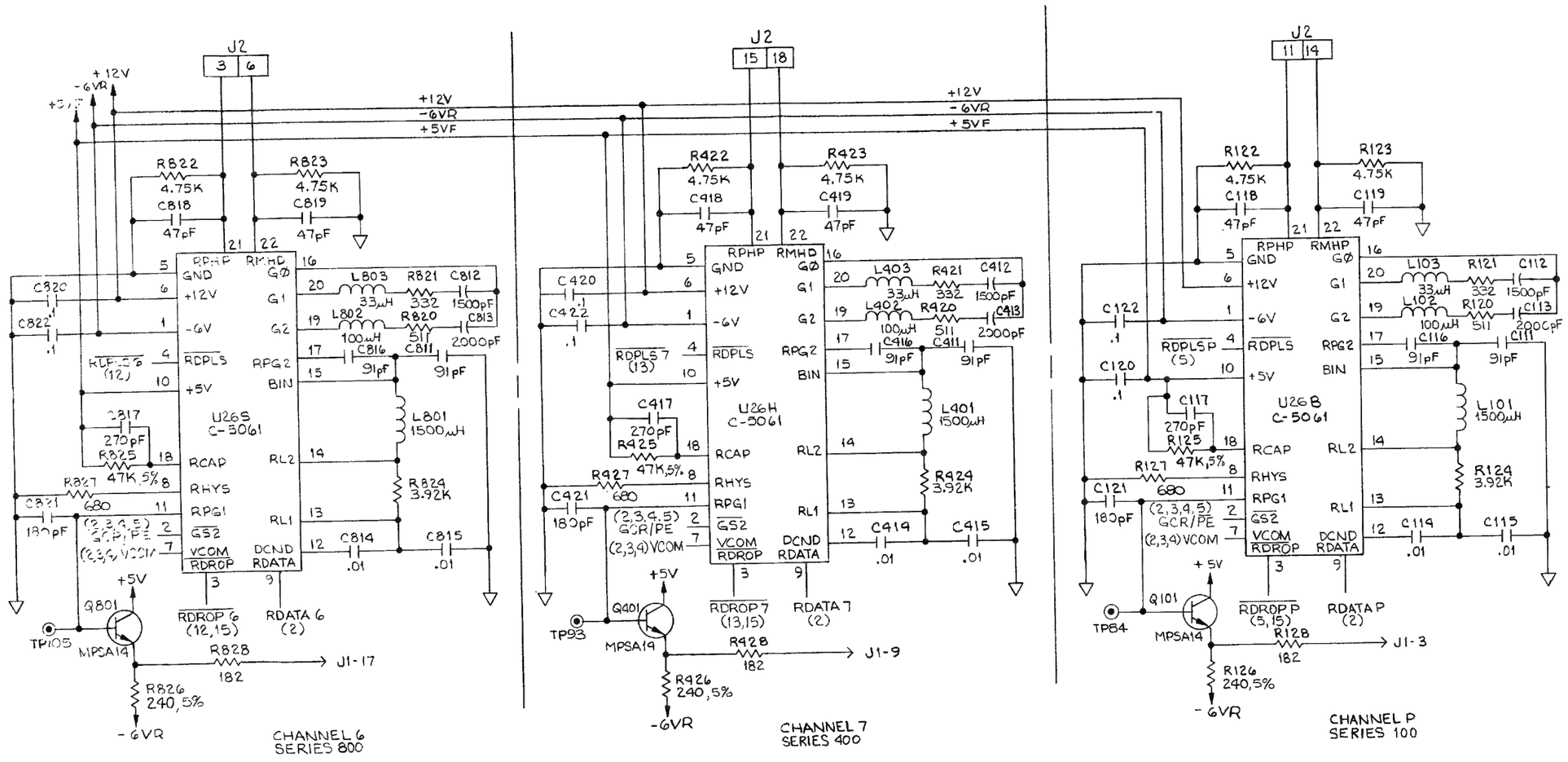
DATA BOARD

Schematic No. 6



DATA BOARD

Schematic No. 6



DATA BOARD

Schematic No. 6

PHASE LOCK LOOP

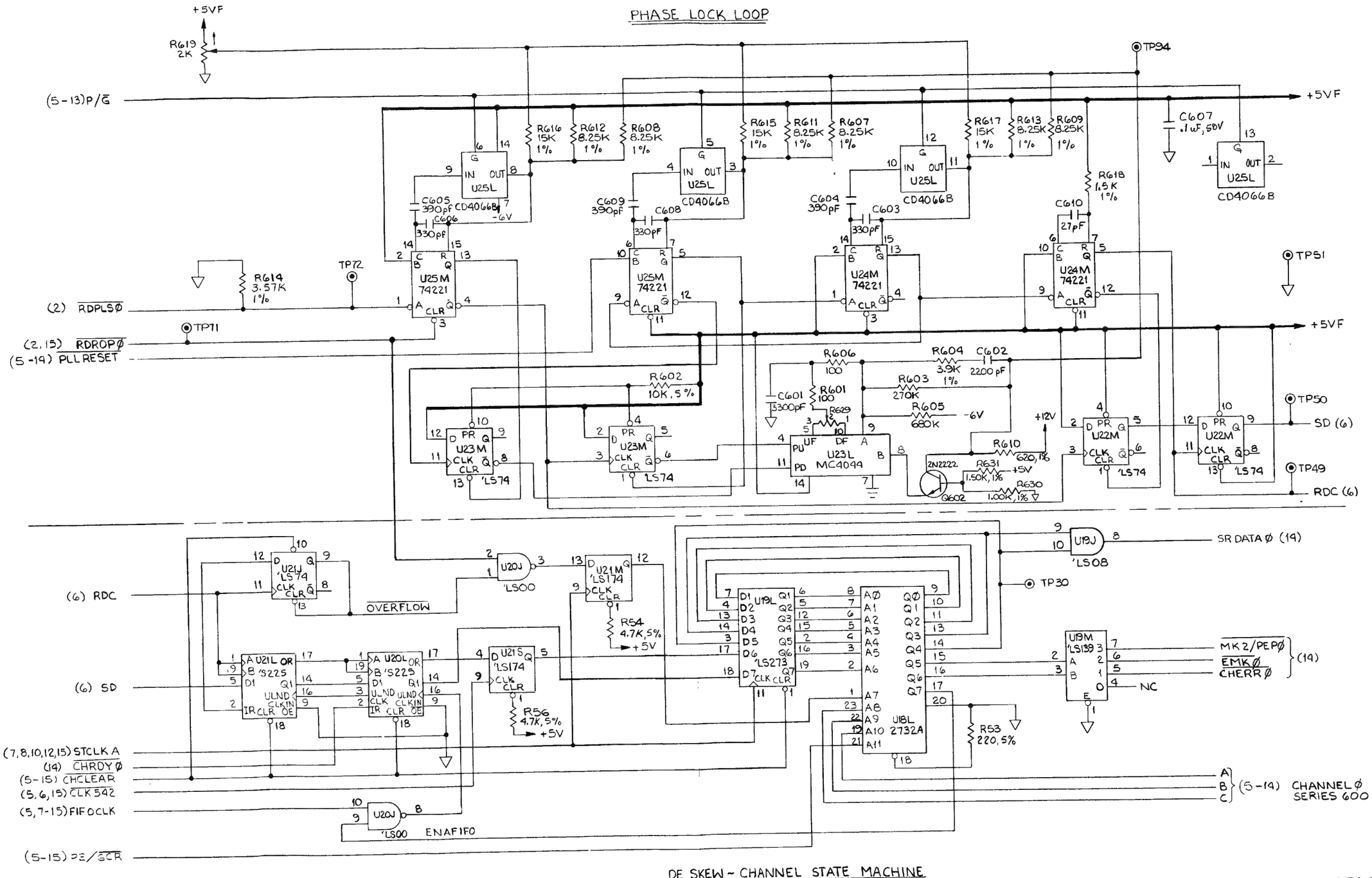
+5VF
R119 2K
(6-13) P/G
(2,3,4) [illegible] PE
(5-15) PE/AGR
(5) RDPLSP
(2,13) RDROPP
(6-[illegible]) PLL RESET
R59 1.5K 5%
R60 4.7K 5%
Q3 2N2907A
R58 4.7K, 5%
Q4 2N2222
R61 22K 5%
- 6 V
R62 4.7K 5%
-6V
R114 3.57K 1%
TP62
TP61
R116 15K 1%
R112 8.25K 1%
R108 8.25K 1%
C105 390pF
C106 330pF
U25A CD4066B
-6V
C109 390pF
C108 330pF
R115 15K 1%
R111 8.25K 1%
R107 8.25K 1%
C104 390pF
C103 330pF
R117 15K 1%
R113 8.25K 1%
R109 8.25K 1%
R118 1.5K 1%
C110 27pF
C107 .1uF, 50V
TP82
TP36
U25B 74221
U24B 74221
R102 10K, 5%
U23B 'LS74
R106 100
R104 3.9K
C102 22.00pF
R103 270K
C101 3300pf
R101 100
R129 Pot
R105 680K
-6V
+12V
U23A MC4044
R110 620
R131 1.50K, 1%
+5V
R130 1.00K, 1%, 1/4W
Q102 2N2222
U22B 'LS74
TP35
SD(5)
TP34
RDC(5)

(5, RDC
(5) SD
(2,9,11,13,14,15 STCLK 3
(14, CHRCYP
(3,13, [illegible]CLEAR
(2,6,[illegible] 7532
(6-15, [illegible]
U21B 'LS74
OVERFLOW
U20B 'LS00
U21D 'LS174
R48 4.7K, 5%
+5V
U21A 'S225
U20A 'S225
U21G 'LS174
R51 4.7K, 5%
+5V
U20B 'LS00 ENAFIFO
U19A 'LS273
U18A 2732A
R45 220, 5%
U19B 'LS08
SRDATAP (14)
TP24
U19D 'LS139
MK2/PEPP
EMK P
CHERR P
(14)
NC
A
B
C
(5-14)
CHANNEL P SERIES 100

DE SKEW - CHANNEL STATE MACHINE

DATA BOARD
Schematic No. 6

PHASE LOCK LOOP



DE SKEW - CHANNEL STATE MACHINE

DATA BOARD

Schematic No. 6

PHASE LOCK LOOP

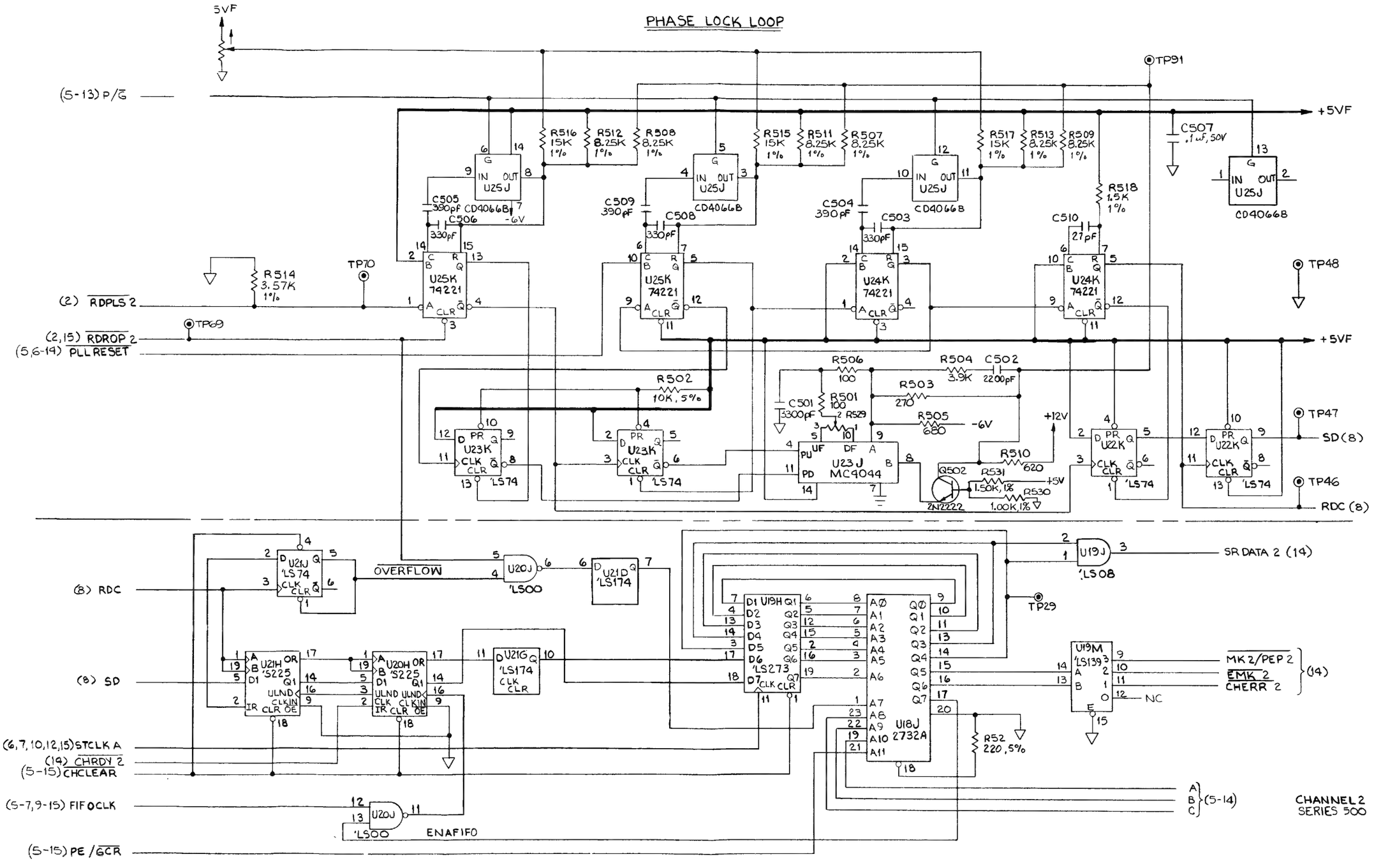
+5VF
R919 2K
(5-13) P/G
+5VF
TP103
R916 15K 1%
R912 8.25K 1%
R908 8.25K 1%
R915 15K 1%
R911 8.25K 1%
R907 8.25K 1%
R917 15K 1%
R913 8.25K 1%
R909 8.25K 1%
C907 .1uF,50V
R918 1.5K 1%
C905 390pF
C906 330pF
C909 390pF
C908 330pF
C904 390pF
C903 330pF
C910 27pF
U25T CD4066B
-6V
R914 3.57K 1%
TP78
TP77
TP60
(2) RDPLS1
(2,15) RDROP1
(56-14) PLLRESET
U25U 74221
U24U 74221
+5VF
R902 10K 5%
R906 100
R904 3.9K
C902 2200pF
R903 270K
C901 3300pF
R901 100
R929 10
R905 680
-6V
+12V
R910 620
2N2222
R931 1.50K,1%
+5V
R930 1.00K,1%
Q902
U23T MC4044
U23U 'LS74
U22U 'LS74
TP59
SD (7)
TP58
RDC (7)

(7) RDC
(7) SD
(6,8,10,12,15) STCLK A
(14) CHRDY1
(5-15) CHCLEAR
(5,6,8-15) FIFOCLK
(5-15) PE/GCR
U21U 'LS79
U20U 'LS00
U21M 'LS174
OVERFLOW
U21T 'S225
U20T 'S225
U21S 'LS174
U20U 'LS00
ENAFIFO
U19T 'LS273
U18T 2732A
R57 220, 5%
U19P 'LS08
SR DATA 1 (14)
TP117
U18U 'LS139
MK2/PEP1
EMK1
CHERR1
(14)
NC
A
B
C
(5-14)
CHANNEL1
SERIES 900

DE SKEW - CHANNEL STATE MACHINE

DATA BOARD
Schematic No. 6

PHASE LOCK LOOP



DE SKEW - CHANNEL STATE MACHINE

DATA BOARD
Schematic No. 6

PHASE LOCK LOOP

+5VF
R219 2K
(5-13) P/G
TP110
+5VF
R216 15K 1%
R212 8.25K 1%
R208 8.25K 1%
R215 15K 1%
R211 8.25K 1%
R207 8.25K 1%
R217 15K 1%
R213 8.25K 1%
R209 8.25K 1%
C207 .1uF, 50V
R218 1.5K 1%
U25C CD4066B
C205 390pF
C206 330pF
C209 390 pF
C208 330pF
C204 390 pF
C203 330pF
C210 27pF
-6V
R214 3.57K 1%
TP64
TP63
TP39
(3) RDPLS 3
(3,15) RDROP 3
(5-14) PLLRESET
U25D 74221
U24D 74221
+5VF
R202 10K, 5%
R206 100
R204 3.9K
C202 2200pF
R203 270K
C201 3300pF
R201 100
R229 10
R205 680K
-6V
+12V
R210 620
R231 1.50K, 1%
R230 1.00K, 1%
+5V
Q202 2N2222
U23D 'LS74
U23C MC4044
U22D 'LS74
TP38
SD (9)
TP37
RDC (9)

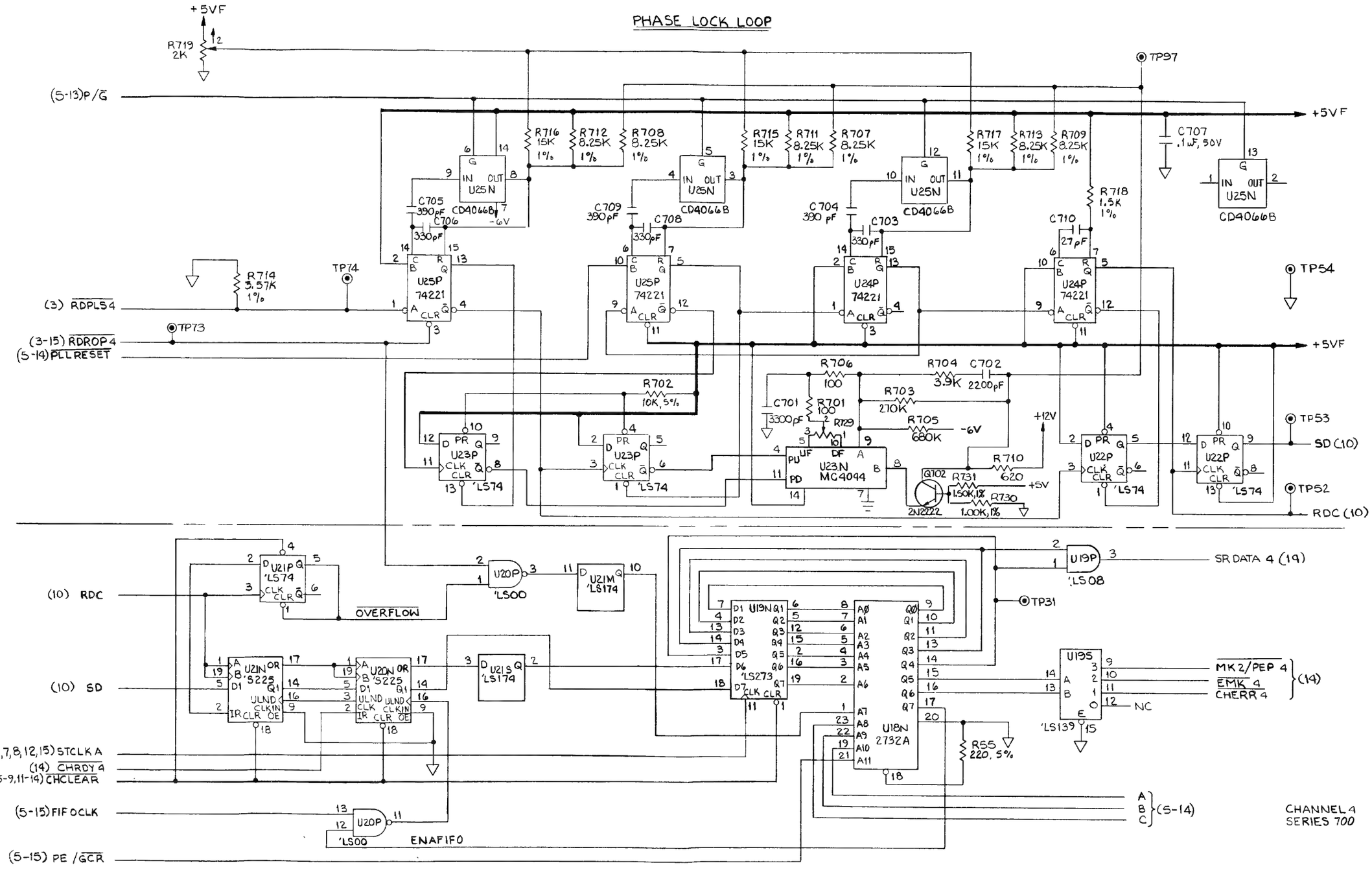
(9) RDC
(9) SD
(5,9,11,13,14,15) STCLK B
(14) CHRDY 3
(5-15) CHCLEAR
(5-15) FIFOCLK
(5-15) PE /GCR
U21B 'LS74
U21C OR 5225
U20C OR 5225
U20B 'LS00
U21D 'LS174
U21G 'LS174
OVERFLOW
ULND CLKIN IR CLR OE
U19C 'LS273
U18C 2732A
R47 220, 5%
U19B 'LS08
SR DATA 3 (19)
TP26
U19D 'LS139
MK 2/PEP 3
EMK 3
CHERR 3
(19)
NC
A
B
C
(5-14)
U20B 'LS00
ENAFIFO

DE SKEW - CHANNEL STATE MACHINE

CHANNEL 3
SERIES 200

DATA BOARD
Schematic No. 6

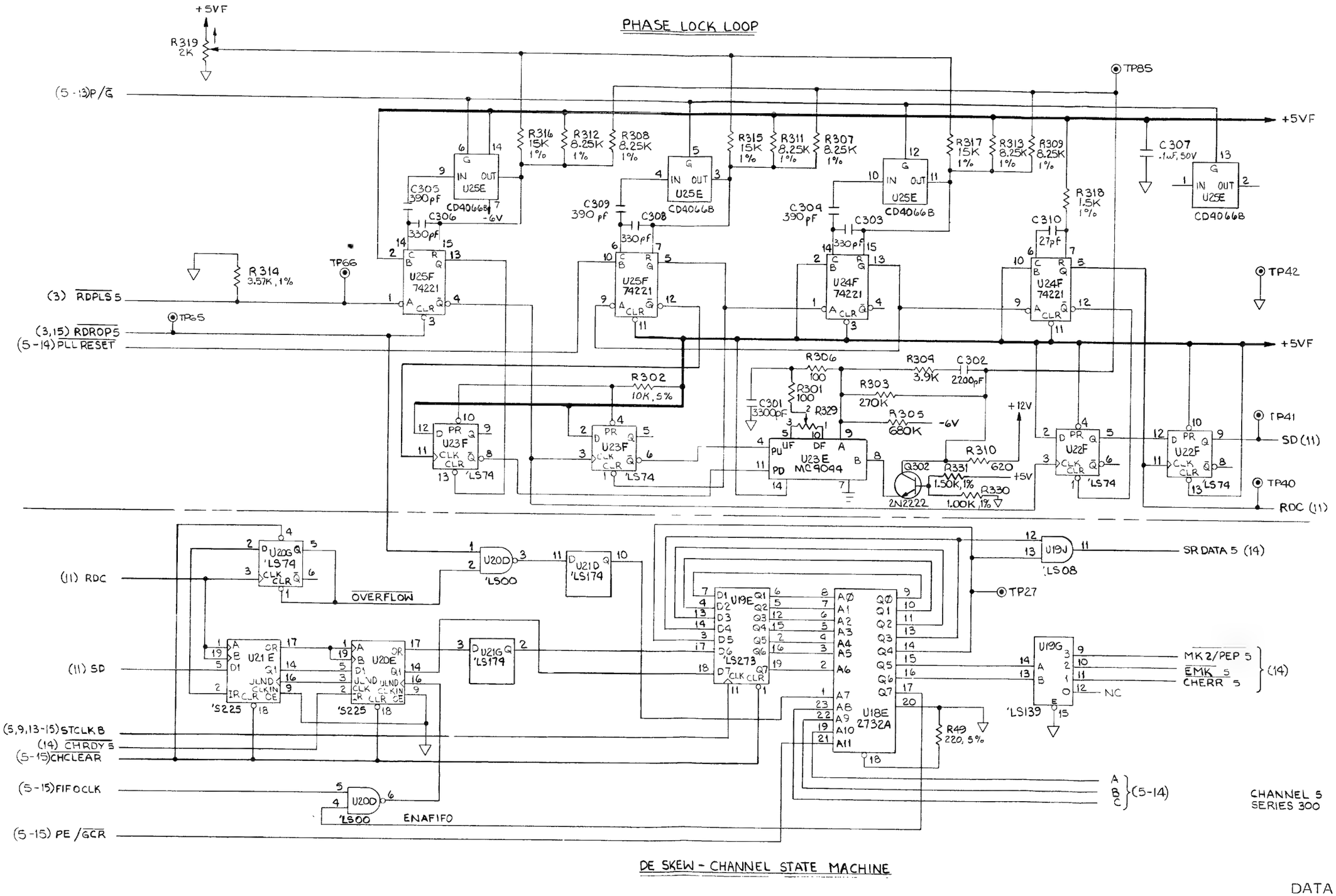
PHASE LOCK LOOP



DE SKEW - CHANNEL STATE MACHINE

DATA BOARD
Schematic No. 6

PHASE LOCK LOOP

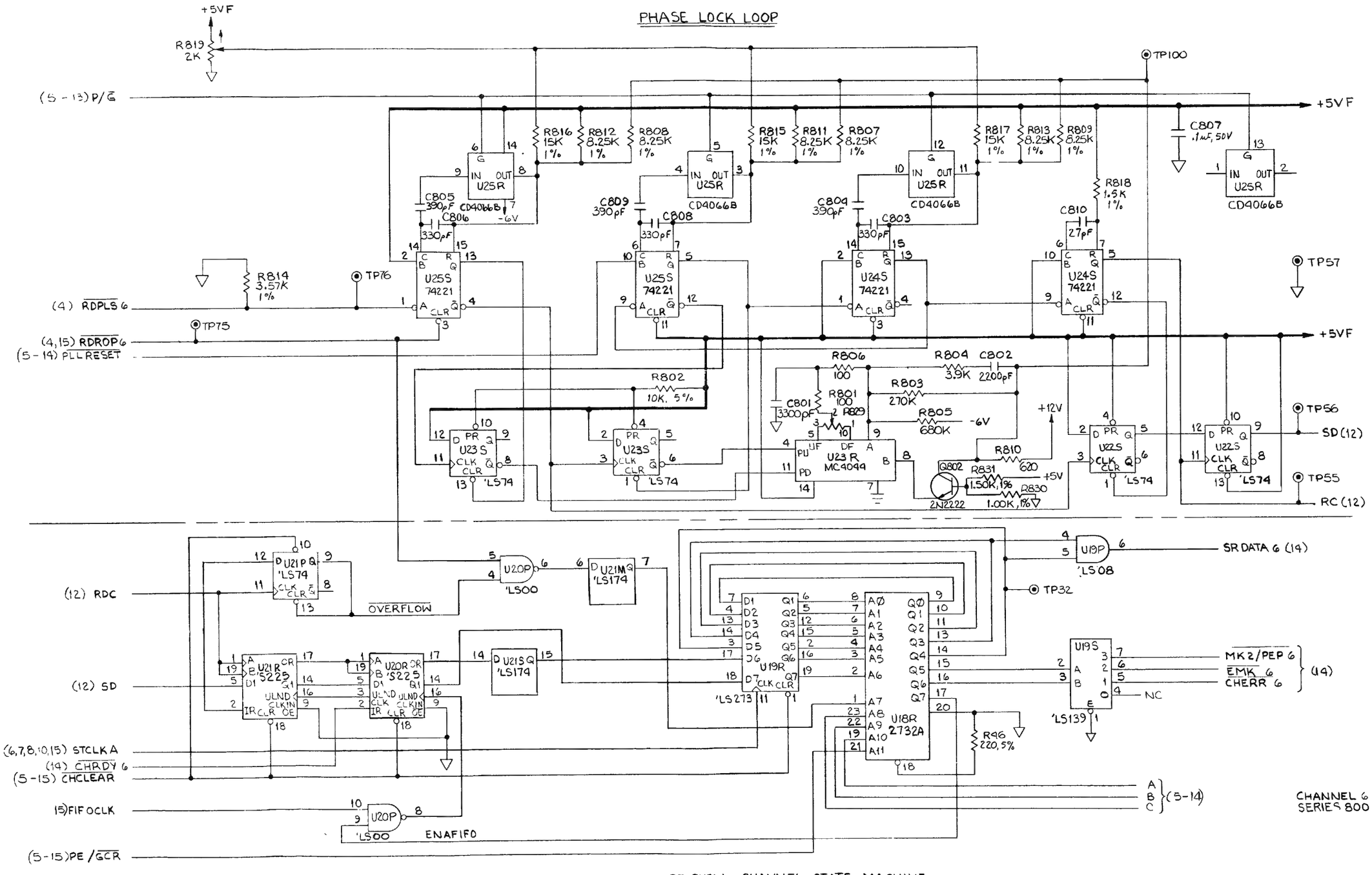


DE SKEW - CHANNEL STATE MACHINE

DATA BOARD

Schematic No. 6

PHASE LOCK LOOP



DE SKEW - CHANNEL STATE MACHINE

DATA BOARD
Schematic No. 6

PHASE LOCK LOOP

+5VF
R419 2K
(5-12) P/G
TP88
+5VF
R416 15K 1%
R412 8.25K 1%
R408 8.25K 1%
R415 15K 1%
R411 8.25K 1%
R407 8.25K 1%
R417 15K 1%
R413 8.25K 1%
R409 8.25K 1%
C407 .1 uF, 50V
R418 1.5K 1%
C410 27pF
C405 390pF
C406 330pF
C409 390pF
C408 330pF
C404 390pF
C403 330pF
U25G CD4066B
-6V
R414 3.57K 1%
TP68
TP67
(4) RDPLS 7
(4,15) RDROP 7
(5-14) PLLRESET
U25H 74221
U24H 74221
TP45
+5VF
R402 10K, 5%
R406 100
R403 270K
R404 3.9K
C402 2200pF
C401 3300pF
R401 100
R405 680K
-6V
+12V
U23H 'LS74
U23G MC4044
R410 620
Q402 2N2222
R431 1.50K, 1%
R430 1.00K, 1%
+5V
U22H 'LS74
TP44
SD (13)
TP43
RDC (13)

(13) RDC
U20S LS74
OVERFLOW
U20D LS00
U19J LS08
SR DATA 7 (14)
TP28
(14) CHRDY 7
(13) SD
U21F OR S225
U20F OR S225
U21G LS174
U19F LS273
U18F 2732A
U19G 'LS139
MK2/PEP 7
EMK 7
CHERR 7
(14)
NC
R50 220, 5%
U21M LS174
(5-15) CHCLEAR
(5-15) FIFOCLK
U20D LS00
ENAFIFO
A
B
C
(5-14)
(5-15) PE/GCR
(5,9,11,13,15) STCLK B

DE SKEW - CHANNEL STATE MACHINE

CHANNEL 7
SERIES 400

DATA BOARD
Schematic No. 6

DATA BOARD

Schematic No. 6

CLOCK GENERATION LOGIC

BLOCK DETECTION

DATA BOARD

Schematic No. 6

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CacheTape® Unit
Theory of Operation

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